A CHARACTERIZATION OF BURIED OXIDE LAYERS FORMED BY OXYGEN IMPLANTATION

By

FREDERICK T. BRADY

A DISSERTATION PRESENTED TO THE GRADUATE SCHOOL
OF THE UNIVERSITY OF FLORIDA IN PARTIAL FULFILLMENT
OF THE REQUIREMENTS FOR THE DEGREE OF
DOCTOR OF PHILOSOPHY

UNIVERSITY OF FLORIDA
1991

ACKNOWLEDGEMENTS

Working towards a Ph.D degree is much like a quest – although it is essentially a solitary project, one is pushed on by his teacher and assisted by those he meets on the way. And so, I would like to thank some of those who have helped me.

First and foremost, I would like to thank my advisor, Dr. Li, for giving me the opportunity to pursue graduate research, and for being very supportive of my research efforts. I am also indebted to Wade Krull of Ibis Technology, for whom I worked as an Associate Engineer for two summers, and who particularly assisted on the radiation study portion of this work. In addition, I gratefully acknowledge the financial support of Harris Corporation, the Rome Air Force Development Center, and the Florida High Technology and Industry Council.

Furthermore, I would like to thank Professors Dorothea Burk, Robert Fox, Arnost Neugroshel, and Kevin Jones for serving on my doctoral committee.

Finally, I would like to thank the various students in the lab through the years for many interesting conversations, and for putting up with me during the times I was heavily using the equipment. I would especially like to thank Hung Shen Chen for many valuable discussions.

TABLE OF CONTENTS

page

ACKNOWLEDGEMENTS ii

ABSTRACT v

CHAPTERS

1. INTRODUCTION 1

1.1 Methods of Forming the SOI Materials 2
1.2 Characterization of Defects in SIMOX Materials and Devices 4
1.3 Objective and Approach 6

2. CAPACITANCE-VOLTAGE THEORY FOR SILICON/INSULATOR/SILICON CAPACITORS 9

2.1 The Si/SiO_2 Interface 9
2.2 Derivation of SIS C-V Theory 11
2.3 Application of SIS C-V Theory to Fitting Experimental Curves 15

3. THE EFFECTS OF PROCESSING ON THE PRE-IRRADIATION DEFECT DENSITIES 23

3.1 Low-Temperature Annealed Samples 23
3.2 Samples Annealed at 1285°C 27
3.3 Quick-Turnaround Devices 29
3.4 Summary 32

4. THE EFFECTS OF TOTAL-DOSE IRRADIATION ON THE CHARGE TRAPPING OF THE BURIED OXIDE LAYER 46

4.1 The Interaction Between Ionizing Radiation and the Si/SiO_2 System 47
4.2 Experimental Details 48
4.3 Basic Radiation Response 49

4.4 The Effects of Processing 52
4.5 Summary 58

5. HIGH ELECTRIC FIELD STRESSING OF THE BURIED OXIDE LAYER 87

5.1 Fowler-Nordheim Tunneling 87
5.2 Experimental Details 89
5.3 Results 90
5.4 Discussion 95
5.5 Summary 97

6. THE DUAL-BEAM OPTICAL MODULATION TECHNIQUE 116

6.1 Nondestructive Evaluation Techniques 117
6.2 Theory of the DBOM Technique 119
6.3 Experimental Details 125
6.4 Results 125
6.5 Summary 127

7. CONCLUSIONS 134

REFERENCES 136

BIOGRAPHICAL SKETCH 142

Abstract of Dissertation Presented to the Graduate School
of the University of Florida in Partial Fulfillment of the
Requirements for the Degree of Doctor of Philosophy

A CHARACTERIZATION OF BURIED OXIDE LAYERS FORMED BY OXYGEN IMPLANTATION

By

Frederick T. Brady

May 1991

Chairman: Prof. Sheng S. Li
Major Department: Electrical Engineering

A thin semiconductor film on an insulating layer presents a device structure with a small active volume and greatly reduced junction capacitances. Thus, much research effort has been spent on SOI (silicon-on-insulator) technology in order to facilitate the development of integrated circuits with superior speed, improved radiation hardness, and freedom from latch-up.

Of the many techniques for forming SOI structures, the most advanced is the oxygen implantation technique, known as SIMOX (Separation by IMplantation of OXygen). In this dissertation, the buried oxide layer formed by the SIMOX technique is studied. The charges of the buried oxide are investigated as the parameters of the SIMOX processing are changed, and as the buried oxide is irradiated or stressed with high voltages. In addition, a technique for the nondestructive evaluation of SIMOX material is presented.

Since the buried oxide capacitor includes two silicon/silicon dioxide interfaces, conventional metal-oxide-semiconductor (MOS) capacitance-voltage theory cannot be

used. Instead, MOS theory is modified to extend to two interfaces. The approach developed consists of fitting theoretical high frequency C-V curves to the measured curves.

The results show that the best quality material is obtained with an oxygen implant dose of 1.8×10^{18} cm^{-2}, and a high anneal temperature. Choosing the anneal time involves a tradeoff, as longer anneals reduce the post-irradiation charge trapping, but increase the pre-irradiation fixed oxide charge density. Some interesting results were obtained in the radiation study. An increase in the film donor density with X-ray dose was discovered. In addition, it was shown that very few interface states were generated by irradiation.

The high electric field stress studies showed that multiple oxygen implant samples were more resistant to stress than were single implant samples. All of the samples were seen to have low threshold fields for electron injection.

Finally, a contactless technique was developed to measure the recombination lifetime of SOI substrates. The transmission of infrared light through the test wafer is measured as it is modulated by free carriers generated by a short wavelength light source. The lifetime is calculated from the magnitude of the modulation.

CHAPTER 1
INTRODUCTION

This dissertation is the result of a research project whose objective was to develop techniques suitable for characterizing the oxide charge and interface traps of buried oxide layers, and to analyze buried oxide layers using these techniques. A second objective was to develop techniques for the rapid evaluation of SOI material.

The idea of fabricating semiconductor devices in a thin Si film on an insulating substrate is attractive for several reasons. First of all, since the source and drain can be fully bottomed, the area of the p-n junctions is greatly reduced, thus greatly reducing the junction leakage. Decreasing the junction area also minimizes the junction capacitances. This results in faster devices. The smaller device volume also has several benefits. The most important of these is a decrease in the sensitivity of devices to single event and transient upset phenomena. Most of the electron-hole pairs generated by ionizing radiation will be generated in the substrate. Since the devices in the active layer are separated from the substrate by an insulating layer, these excess carriers will not be able to upset the logic states of devices in the film. Another benefit of the smaller volume is a reduced diffusion current, which allows operation at high temperatures. An additional benefit of the SOI device structure is the elimination of latch-up. Latch-up is the formation of parasitic transistors or silicon-controlled rectifiers between neighboring devices. In bulk Si technology, neighboring devices are isolated by p-n junctions. Under certain conditions, such as radiation or electrostatic discharge, the isolating junction can become forward biased. In SOI technology, devices sit on an insulating layer. Thus, neighboring devices can easily be isolated from one another.

1.1 Methods of Forming the SOI Materials

Because of the above advantages, researchers have been investigating silicon-on-insulator (SOI) materials since the mid-1960's. Many different materials were investigated for use as the insulating layer, but problems in achieving high quality silicon films were encountered. Eventually, the silicon-on-sapphire (SOS) approach emerged as the technology of choice. The SOS structure consists of a thin Si film grown on a sapphire substrate. However, SOS still has problems with a high defect density in the film and a poor film/sapphire interface. The development of solid phase epitaxy techniques has dramatically improved the quality of the silicon film [1], but material problems remain. In addition, the sapphire substrate is transparent and brittle. These properties make it difficult to use SOS wafers in standard production lines. Because of these problems, SOS circuits have been limited to applications in which radiation hardness is the prime concern.

With the problems of SOS devices, much effort has been spent developing an SOI approach with SiO_2 as the insulating layer. A number of promising approaches have been developed. They include the recrystallization of polysilicon, BESOI (bond and etchback SOI), and SIMOX (Separation by IMplantation of OXygen). These techniques are described below.

In the recrystallization procedures, the first step is the growth of a thermal oxide on the silicon wafer. If the recrystallization is to be seeded, vias are etched in the oxide to the Si substrate. Next, polysilicon is deposited on the oxide. The substrate is then heated, and a heat source is passed over/on the polysilicon. A variety of heat sources have been used, such as lasers [2],[3], electron beams [4], lamps [5], and graphite heaters [6]. The sweep rate and substrate temperature depend on the type of heat source. After recrystallization, grain boundaries or subboundries remain. Between boundaries, the Si film quality is excellent. The primary application for the recrystallization techniques appears to be three dimensional circuits.

The BESOI technique proceeds as follows. First, a thermal oxide is grown on a handle wafer. Next, a second Si wafer is brought close to the handle wafer, and the wafers oxidized together. The second wafer is then polished and etched down to the desired film thickness. Due to a lack of control over the etching rates, it is difficult to achieve uniform film thicknesses in the submicron range. An additional problem is the presence of voids between the two wafers. A recent development is the use of backside implants to create n^+ or p^+ etch stops. With the addition of a second front side etch stop implant, bonded wafers with very uniform (+/- 10 nm) Si films have been fabricated with down to thicknesses of 580 nm [7]. However, at this time, the bonded wafer approach appears to best suited for bipolar applications, which require relatively thick, high quality films.

The technique regarded as the most promising is the SIMOX technique [8]. The SIMOX process consists of implanting a very high dose of oxygen (typically 1.5 – 2.2×10^{18} cm^{-2}) into a silicon wafer, followed by a high temperature anneal (at least 1285°C for 6 hours). The lower end of the dose range corresponds to the minimum dose required to form a continuous buried oxide layer [9]. The upper end is determined by the fact that some Si overlayer must remain intact after the implant [10]. Alternately, one can implant a lower dose and perform several sequential implant and anneals. Evidence indicates that the multiple implant approach may be superior to single implants [11]. The usual implant energy is 150-200 keV, and the wafers are typically heated to 500-700°C during the implant from beam heating. The lower bounds of the energy is limited by the need to prevent all of the Si overlayer from being sputtered away or consumed by the oxide. The upper bounds is determined by the practical limitations of ion implanters. The lower bounds of the implant temperature is an important quantity. At lower temperatures, the film/buried oxide interface becomes polycrystalline or amorphous. This damage cannot be annealed out [12,13,14]. Following the implant and anneal, about 0.2 μm of silicon film is left. One can then

grow an epilayer, or proceed with device fabrication. The advantage of the SIMOX technique over the previously discussed techniques is that following the post-implant anneal, the Si is very uniform, and reasonably defect free. At this time, none of the other techniques can match the ultra-thin film uniformity of the SIMOX process.

At this time, a variety of CMOS circuits have been fabricated using the SIMOX process. Examples include 64k SRAMs [15,16,17] and CMOS prescalar circuits operating at 6.2 GHz [18]. Under development are 256k SRAMS.

1.2 Characterization of Defects in SIMOX Materials and Devices

The process of implanting such a high dose of ions creates a highly damaged structure. The primary defects are dislocations and oxide precipitates in the Si film, a rough film/buried oxide (F/O) interface, and Si precipitates in the oxide [19]. In addition, the insides of the implanter are scoured by the implanting beam, leading to the implantation of metal contaminants [20]. The high temperature anneal significantly reduces the density of these defects, but it does not eliminate them [21]. Furthermore, as discussed below, it may be beneficial to have a certain level of damage. The importance of the various defects depends on the device geometry, which depends in large part on the intended application. There are basically two applications for SIMOX/CMOS circuits: radiation-hardened and advanced VLSI. The geometry for these two applications can in turn be divided into partially depleted (PD) and fully depleted (FD) film. A PD film is partially depleted during device operation, while a FD film is fully depleted during device operation. Although the depletion state of the film depends on the doping and thickness of the film, films thinner than 0.2 μm are generally FD. For VLSI applications, FD films are used. This is due to several advantages unique to FD films, such as increased carrier mobility [22], higher drive currents [23], and a subthreshold slope near the theoretical maximum [24]. However, in FD devices, the threshold voltage of the front gate is coupled to the substrate bias. Thus voltage shifts at the film/buried oxide (F/O) interface are coupled to the front

gate. Thus, it is very important to have a good quality F/O interface. The coupling effect also makes it very challenging to harden FD devices to total dose irradiation. Another difficulty with FD devices is the parasitic bipolar effect. In samples with a high carrier lifetime in the film, majority carriers collect in the body (since there is no body contact). The presence of majority carriers increases the potential in the body, eventually turning on the parasitic bipolar transistor [25]. This can cause breakdown. Thus, the excess carrier lifetime is an important parameter.

The main application of PD devices is radiation hardened circuits. It is difficult to use FD devices in rad hard applications because of the coupling between the front and back gate voltages. Since there is no coupling in PD films, degradation of the back channel only increases the device leakage. Even more than in FD devices, the recombination lifetime is very important in rad-hard PD devices. If the excess carriers generated by radiation are not removed quickly, the parasitic bipolar transistor will turn on.

Finally, for all applications, the minority carrier generation lifetime is an important parameter. This parameter is closely related to the reverse bias leakage of p/n junctions, and so is a good indicator of material quality.

Approaches to characterizing SIMOX material can be divided into analytical methods (TEMs, SIMS, Auger) and electrical methods (transistor parameter extraction, diode measurements). Much analytical work has been published on effect of SIMOX processing on the defects of the film and buried oxide [8–14]. Although these techniques are satisfactory for evaluating the quality of the microstructure and determining the impurity content, they do not indicate the density of electrically active defects. Electrical characterizations of SIMOX material have focused on diode and MOSFET measurements, such as junction leakage [29] and DLTS (deep level transient spectroscopy) [30]. Although these electrical techniques are useful for evaluating defects in the Si film, one can only get a rough idea of the density of interface states

and fixed oxide charge at the F/O interface. No information on the density of defects at the S/O (substrate/buried oxide) interface can be obtained using these techniques. Although the S/O interface is not of great technological importance, comparison of the S/O and F/O interfaces improves the overall understanding of the buried oxide. Thus there is a need to develop a technique that can measure the defect density of the buried oxide. Furthermore, the electrical techniques described above require careful fabrication of test structures, and so are not suitable for quick evaluation of SIMOX material. Several techniques have been applied to SIMOX material for quick evaluation, such as SPV (surface photovoltage) [31] and spectroscopic ellipsometry [32]. However, these techniques give only rough information on the defect density, information only on the microstructure (spectroscopic ellipsometry), or the diffusion length for only the substrate (SPV). Finally, despite the importance of the buried oxide to the radiation hardness of SIMOX devices, very little characterization of the effects of ionizing radiation on the buried oxide layer has been done. The few studies that have been done have primarily centered on analysis of the back-channel transistors. It is difficult to separate the contributions of interface states and fixed oxide charge with MOSFET measurements.

A final point to consider is that the SIMOX process is very different from the thermal or CVD oxide growth process. Thus, SIMOX oxides are essentially a new material, and so need to be studied from the standpoint of scientific interest.

1.3 Objective and Approach

In this study, there are five basic objectives. They are:

1. Develop a technique to measure the interface state and fixed oxide charge densities at both buried oxide interfaces.

2. Use this technique to characterize the effect of SIMOX processing on the defects of the buried oxide.

3. Develop a method for quick-turn evaluation of SIMOX buried oxides.

4. Use the buried oxide characterization technique to study the effects of total dose irradiation on the buried oxide.

5. Develop additional quick-turn/nondestructive techniques for evaluation of SIMOX wafers.

The format of the disseration is as follows.

In Chapter 2, the high frequency C-V theory for the buried oxide capacitor is derived. The chapter begins with the general expression for the capacitance of the Si/SiO_2 interface, then the high frequency approximation is discussed. Finally, the details of the curve fitting are discussed, followed by an example.

Chapter 3 discusses the effects of SIMOX processing on the buried oxide defects, prior to any radiation or high field stressing. First, C-V and C-t measurements are used to characterize samples annealed at low temperatures. The generation lifetime of the film and substrate, as calculated from the C-t measurements are correlated to the C-V measurements. Next, samples annealed at 1285°C are discussed. Again, C-t measurements are correlated to the C-V analysis. Finally, the quick-turnaround fabrication technique is developed, and the approach used to study a batch of wafers implanted together, but given various anneals, and implanted with or without a screen oxide.

In Chapter 4, the effects of radiation on SIMOX buried oxides are discussed. The chapter begins with a review of the basic effects of ionizing radiation on SiO_2. Next, the basic radiation effects of SIMOX oxides are discussed. Finally, the effects of SIMOX processing on the charge trapping are discussed.

Next, high voltage stressing is studied. Both ramped I-V and constant bias stressing are examined. The results are correlated to the radiation effects discussed in Chapter 4. The study focuses on samples annealed at 1285°C for 6 hours.

Following the discussion of bias stress effects, Chapter 6 concerns the development of a nondestructive technique for evaluating thin film SOI wafers. The method, known as the dual beam optical modulation technique, consists of using one light source for pumping up the carrier density, while monitoring the attenuation of the second light by free carrier absorption as it passes through the wafer.

Finally, in Chapter 7, the dissertation is summed up, and the major conclusions given.

CHAPTER 2
CAPACITANCE-VOLTAGE THEORY FOR SILICON/INSULATOR/INSULATOR CAPACITORS

This chapter presents the theoretical background for C-V analysis of SIMOX buried oxide layers. The chapter begins with a description of the various charges found in an oxide layer and its interface. General C-V theory is derived, followed by the high frequency approximation. The generation of the theoretical C-V curve and the curve fitting approach are then discussed.

2.1 The Si/SiO_2 Interface

The SiO_2 layer in semiconductor devices is an amorphous structure, consisting of a random network of four oxygen atoms bonded to one silicon atom. For a high quality Si/SiO_2 interface, the transition from crystalline silicon to stoichometric SiO_2 is atomically sharp. The transition region consists of SiO_x, where x is less than 2. X-ray photospectroscopy (XPS) measurements have found this region to be approximately 10 Å thick [33],[34]. A tail of silicon bonding to only three oxygen atoms extends about 30 Å into the oxide. There are four major types of charges in SiO_2 and at its interface with silicon. These are mobile ionic charge (Q_m), oxide trapped charge (Q_{ot}), fixed oxide charge (Q_f), and interface trapped charge (Q_{it}).

The source of mobile ionic charge is usually sodium or potassium ions, which become mobile at higher temperatures under an electric field. These positively charged ions migrate from the bulk of the oxide to the Si/SiO_2 interface over a period of time, slowly increasing the oxide charge there [35]. Ionic charge is not a factor in semiconductor processing today.

Oxide trapped charges arise from defects in the oxide. These defects can be structural or chemical. The defects, initially neutral, capture electrons or holes to become charged. An example of this is the E' center. The E' center is a silicon atom in the bulk of the oxide that is missing an oxygen bond ($\cdot Si{\equiv}O$). It has been shown to correlate with positive oxide charge following irradiation [36]. Since very little current flows through the oxide layer during normal device operation, the traps usually remain neutral. However, if carriers are injected into the oxide these traps can become charged [37]. The distribution of Q_m and Q_{ot} depends very strongly on the history of the oxide.

Fixed oxide charge may be caused by more than one type of defect. Although 90% of the charge distribution is located within 34 Å of the Si/SiO_2 interface [38], fixed charge is not mobile and is independent of the applied voltage. However, the chemical identity of Q_f has not been established. The value of Q_f is highly dependent on the process used to the create the oxide layer, and on the orientation of the silicon.

Finally, the most common source of interface traps is the P_b center. P_b centers are silicon atoms on the silicon side of the Si/SiO_2 interface bonding to three Si atoms rather than four ($\cdot Si{\equiv}Si$). The dangling bond is an amphoteric trap [39],[40]. As the Fermi level rises from the valence band toward mid gap, the traps capture electrons, becoming neutral. As the Fermi level rises towards the conduction band, the traps accept additional electrons, becoming negatively charged. It is also possible for positive charges near the interface to induce interface traps [38]. The energies of the traps vary continuously throughout the silicon bandgap. Therefore, their probability of trapping an electron is dependent on the applied voltage.

The positions of Q_m, Q_{ox}, Q_f, and Q_{it} in the SIMOX structure are shown in Figure 2.1. The spatial distribution of charge in the oxide cannot be determined from C-V measurements (aside from destructive etch back experiments). One can only measure the centroid of the charge. Thus, in the following derivation, the oxide

charge will be modelled as a sheet of charge at the oxide interfaces. For good quality thermal oxides, this is a good assumption, as Q_f and Q_{ox} are located very near the oxide interfaces.

2.2 Derivation of SIS C–V Theory

The energy band diagram for the buried oxide capacitor (BOXCAP) and the equivalent capacitance are shown in Figs. 2.2 and 2.3, respectively. In this example, both the film and substrate are assumed to be n-type. The derivation of the high frequency C-V characteristics is based on the following assumptions:

1. Minority carriers do not respond to the ac signal.
2. Doping near the oxide interfaces is uniform.
3. Q_f can be represented as a sheet of charge.
4. Q_{it} does not respond to the ac signal.
5. The distribution of interface traps across the bandgap can be modelled as approximately U-shaped.
6. Interface traps in the upper half of the bandgap are acceptor-like (negative when filled), and traps in the lower half of the bandgap are donor like (neutral when filled).
7. The film is never fully depleted.
8. There is no dielectric constant grading between the buried oxide and the silicon layers.

If the substrate is grounded, and a voltage applied to the film, part of the voltage drop will be across the film (S1), part across the oxide, and part across the substrate

(S2). There is also a built-in potential caused by the work function difference between the film and substrate, denoted by W_{12}. The applied voltage can then be expressed as

$$V_a = V_{S1} + V_{ox} + V_{S2} + W_{12} \tag{1}$$

Assuming the voltage drop across the bulks of the film and substrate to be negligible, V_{S1} and V_{S2} are equal to the silicon band bending at the interfaces, and denoted by ψ_{s1} and ψ_{s2}, respectively. The work function difference between two semiconductors, where S2 is grounded, is [41]

$$W_{12} = \chi_1 + \frac{E_{g1}}{2q} - \phi_{b1} - (\chi_2 + \frac{E_{g2}}{2q} - \phi_{b2}) \tag{2}$$

In the above equation, χ is electron affinity, E_g is energy gap, and q is elementary charge. Since both semiconductors are silicon, $\chi_1 = \chi_2$ and $E_{g1} = E_{g2}$. The expression for work function simplifies to

$$W_{12} = \phi_{b2} - \phi_{b1} \tag{3}$$

In analogy to a parallel-plate capacitor, the voltage across the oxide is equal to Q_{ox}/C_{ox}. The oxide capacitance is given by C_{ox}, while Q_{ox} is the charge stored by the capacitor. Since the charge at the S1 interface must be equal and opposite to the charge at the S2 interface, Q_{ox} can be written in terms of the charges at either interface. If the S1 interface is taken as $x = 0$, then

$$Q_{ox} = Q_{s1} + Q_{t1} + (1 - \bar{x}/d_{ox})Q_f = -Q_{s2} - Q_{t2} - \bar{x}Q_f/d_{ox} \tag{4}$$

In the above equation, Q_s is the charge at the surface of silicon, Q_t is the interface trap charge, $\bar{x}$ is the average position of oxide charge distribution, and d_{ox} is the oxide thickness. A 1 or 2 in the subscript refers to S1 or S2 respectively. If Q_f is represented as a sheet of charge at $x = 0$ and at $x = 1$, then

$$Q_{f1} = (1 - \bar{x}/d_{ox})Q_f \tag{5}$$

and

$$Q_{f2} = \bar{x}Q_f/d_{ox} \tag{6}$$

Eq. (1) can then be written in terms of the charge at the S2 interface as

$$V_a = -\psi_{s1} - \frac{Q_{s2} + Q_{t2} + Q_{f2}}{C_{ox}} + \psi_{s2} + W_{12} \tag{7}$$

Alternatively, Eq. (1) can be written in terms of charge at the S1 interface:

$$V_a = -\psi_{s1} + \frac{Q_{s1} + Q_{t1} + Q_{f1}}{C_{ox}} + \psi_{s2} + W_{12} \tag{8}$$

The equivalent circuit for the BOXCAP can be derived in the following manner. When a small amplitude, time varying voltage is applied, the amount of charge at the silicon surfaces and the charge trapped at the oxide interfaces will change. The silicon surface and the interface traps can be viewed as storing charge, and so having a capacitance. An expression for surface capacitance is derived below.

2.2.1 General Result [38]

The differential capacitance C_s is defined as

$$C_s(\psi_s) = -\frac{dQ_s}{d\psi_s} \tag{9}$$

The relationship between Q_s and ψ_s is

$$Q_s = Sgn(-v_s)\frac{\epsilon_s V_T}{L_i}F(v_s) \tag{10}$$

In the above equation, Sgn(-v_s) is the negative of the sign of v_s, ϵ_s is the dielectric constant for silicon, V_T is the thermal voltage, $F(v_s)$ is the normalized electric field, and L_i is the intrinsic Debye length for silicon. The normalized band bending, v_s, is equal to ψ_s/V_T. The electric field is equal to

$$F(v_s) = ([-kv_s - 1 + \exp(kv_s) + (\frac{n_i}{N})^2\exp(-kv_s)]\frac{N}{n_i})^{1/2} \tag{11}$$

In Eq. (11), n_i is the intrinsic carrier concentration, N is doping density, and k is equal to 1 for n-type silicon and -1 for p-type silicon. The expression for C_s then

becomes

$$C_s = \frac{C_{fbs}[k\exp(kv_s) - k(n_i/N)^2\exp(-kv_s) - 1]}{(2[-kv_s - 1 + \exp(kv_s) + (n_i/N)^2\exp(-kv_s)])^{1/2}} \tag{12}$$

C_{fbs} is the surface capacitance for $v_s = 0$. It is equal to

$$C_{fbs} = \frac{\epsilon_s}{L_d} \tag{13}$$

where L_d is the extrinsic Debye length. Similarly, the differential capacitance of interface traps is defined as

$$C_t(\psi_s) = -\frac{dQ_t}{d\psi_s} \tag{14}$$

The amount of trapped charge is related to the band bending by

$$Q_t = q\int_{E_v}^{E_c}[D_{tD}(E)f_D(E) - D_{tA}(E)f_A(E)]dE \tag{15}$$

The quantities $f_D(E)$ and $f_A(E)$ are the Fermi distribution functions for donor traps and acceptor traps, respectively, given by

$$f(E) = [1 + g\exp(k[\phi_b + \psi_s - \phi_t]/V_T)]^{-1} \tag{16}$$

where ϕ_b is the bulk potential and ϕ_t is the trap energy of interest. The quantity k is equal to 1 for donor traps and -1 for acceptor traps. The variable g is the degeneracy factor, equal to 1/2 for donor traps and 1/4 for acceptor traps. The quantities $D_{tD}(E)$ and $D_{tA}(E)$ represent the distribution of donor and acceptor traps respectively, in the silicon bandgap. To a first order approximation, only traps within a few V_T of the Fermi level contribute capacitance. Therefore

$$C_{it}(\psi_s) = qD_{tA}(E) + qD_{tD}(E) \tag{17}$$

The total capacitance of the BOXCAP is

$$\frac{1}{C_T} = \frac{1}{C_{s1} + C_{t1}} + \frac{1}{C_{ox}} + \frac{1}{C_{s2} + C_{t2}} \tag{18}$$

2.2.2 High frequency approximation

If the ac signal is of high enough frequency, minority carriers and interface traps will not respond. This frequency is approximately 1 KHz for minority carriers, and 100 MHz for interface traps near the band edges. However, 1 MHz is usually high enough for traps over most of the bandgap. As a result, minority carriers and interface traps contribute no capacitance. They do follow the dc bias, and so affect neutrality requirements. Equation (12) for C_s must be changed to account for the lack of minority carrier response. It becomes

$$C_s = \frac{C_{fbs}[k\exp(kv_s) - 1]}{[2(-kv_s - 1 + \exp(kv_s))]^{1/2}} \tag{19}$$

A second-order effect must be taken into account at this point. This is the capacitance caused by the spacial rearrangement of minority carriers at the surface. Although the area density of minority carriers does not change in response to the ac signal, there is a volume change. This volume change affects the width of the depletion layer. Neglecting this effect can cause a 7% error in estimating the depletion capacitance, which in turn causes an error in estimating doping concentration. This error can be made less than 1% by choosing a certain surface potential to minimize the error. From Nicollian and Brews [38], this surface potential is

$$\psi_m = \psi_L - 0.75V_T \tag{20}$$

where ψ_L is the Lindner potential, described later. The band bending is restricted to being less than ψ_L. The expression for total capacitance simplifies to

$$\frac{1}{C_T} = \frac{1}{C_{s1}} + \frac{1}{C_{ox}} + \frac{1}{C_{s2}} \tag{21}$$

2.3 Application of SIS C-V Theory to Fitting Experimental Curves

The theoretical C-V curve is generated from data obtained experimentally. The critical information is doping density at both interfaces, oxide capacitance, and oxide

area. From this information, an ideal C-V can be generated. To better fit the experimental curve, Q_f and Q_{it} can be added to the model. The process of curve fitting is shown in Figure 2.4. The details for generating the C-V curve are described below.

The oxide capacitance is determined by measuring a capacitor with a film and substrate of different dopant type. For example, if the film is n-type and the substrate is p-type and grounded, a sufficiently negative voltage applied to the film will cause both interfaces to be in accumulation. This means that C_{s1} and C_{s2} are much greater than C_{ox}. Thus

$$C_T = C_{ox} \tag{22}$$

Alternately, the inversion capacitance can be measured at very low frequencies or with a bright light shining on the samples. The thickness of the oxide is then calculated from

$$d_{ox} = \frac{\epsilon_{ox} A}{C_{ox}} \tag{23}$$

where A is the area of the capacitor. The doping concentrations can be obtained from the strong inversion capacitance of each interface. For a BOXCAP with both semiconductor layers of the same dopant type, when one interface is far into depletion, the other interface is in accumulation, and its capacitance can be neglected. The total capacitance is then

$$\frac{1}{C_T} = \frac{1}{C_{dep}} + \frac{1}{C_{ox}} \tag{24}$$

where

$$C_{dep} = \frac{\epsilon_s A}{W} \tag{25}$$

In Eq. (25), W is the width of the depletion layer. As the magnitude of the applied voltage is increased, the depletion width increases (to maintain neutrality), lowering the total capacitance. However, the minority carrier density also increases, and eventually the silicon surface responds to an increase in voltage by increasing the minority carrier density rather than increasing the depletion width. Thus, there is a capacitance minimum when the minority carrier density approximately equals the

doping density. The surface potential at this point is given by the Lindner potential [38], and is equal to

$$\psi_L = V_T[2.1\ln(\frac{N}{n_i}) + 2.08] \tag{26}$$

The maximum depletion width is then

$$W_{max} = \sqrt{\frac{2\epsilon_s\psi_L}{qN}} \tag{27}$$

From the measured curve

$$W_{max} = (\epsilon_{ox}A)(\frac{1}{C_{min}} - \frac{1}{C_{ox}}) \tag{28}$$

where C_{min} is the minimum capacitance. From the last two equations:

$$N = \frac{2\epsilon_s\psi_L}{q}[\epsilon_{ox}A(\frac{1}{C_{min}} - \frac{1}{C_{ox}})]^{-2} \tag{29}$$

Using the above equation, the doping density can be calculated for both interfaces. Now, the capacitance as function of voltage can be found.

Since neutrality is required, from Eq. (4)

$$Q_{s1} + Q_{t1} + Q_n + Q_{s2} + Q_{t2} + Q_{f2} = 0 \tag{30}$$

If v_{s2} is assumed to be known, then v_{s1} can be found using a zero finding algorithm, with v_{s1} as the unknown. Values for Q_f and D_{it} are picked by the user. Once the function has been zeroed, the gate voltage V_a is calculated from Eq. (7) or Eq. (8). With the band bending at each interface known, the surface capacitances can be calculated from Eq. (19). The total capacitance for the given surface potentials is then

$$\frac{1}{C_T(v_{s1}, v_{s2})} = \frac{1}{C_{s1}(v_{s1})} + \frac{1}{C_{ox}} + \frac{1}{C_{s2}(v_{s2})} \tag{31}$$

In Figure 2.4, the procedure of fitting theoretical C-V curves to experimental C-V curves is shown. First, the ideal C-V curve is compared to the measured C-V curve. Then, as discussed above, oxide thickness and epilayer and substrate doping are

calculated from the measured curve. When fixed oxide charge is taken into account, the fit improves, but the measured curve is stretched out relative to the theoretical curve. Finally, when interface trapped charge is accounted for, the theoretical curve fits the measured curve well. It is noted that other groups have generated theoretical C-V curves for the silicon-oxide-silicon structure [42,43]; however, this is the first work to actually extract parameters from the measured C-V curve.

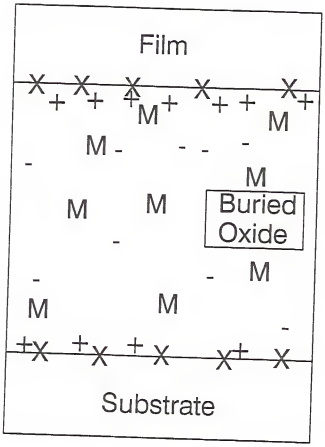
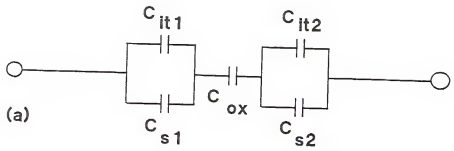


Figure 2.1. A sketch of the SOI structure, showing the possible positions of the various oxide charges. The meaning of the various symbols is as follows: X's represent interface states, +'s represent fixed oxide charge, -'s are oxide trapped charge, and the M's are mobile ion charge.



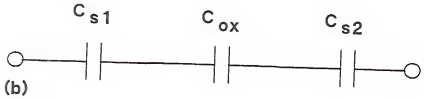


Figure 2.2. The equivalent capacitances of the buried oxide capacitor for (a) low frequency measurements and (b) the high frequency approximation.

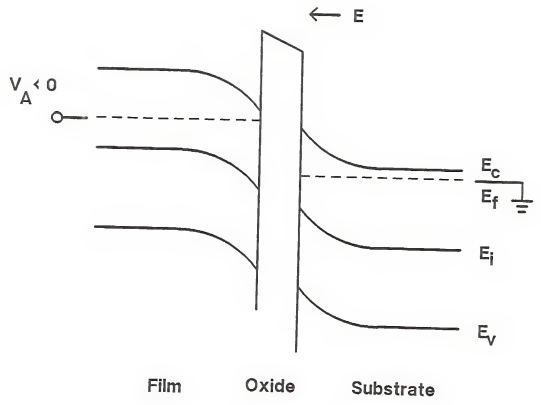


Figure 2.3. The energy band diagram for the buried oxide capacitor, for the case of the substrate grounded and a negative bias applied to the film.

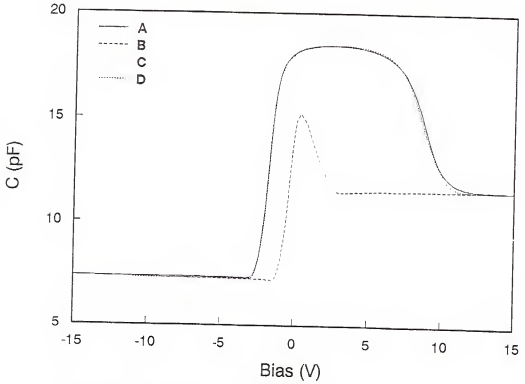


Figure 2.4. An example of the curve fitting approach. The curves are as follows: 'A' is the measured curve; 'B' is the ideal fit; 'C' is the fit with fixed oxide charge but no interface traps; and 'D' is the final fit, with both fixed oxide charge and interface traps taken into account.

CHAPTER 3
THE EFFECTS OF PROCESSING ON THE PRE-IRRADIATION DEFECT DENSITIES

In this chapter, the effects of SIMOX processing on the defects of the buried oxide layer are investigated. The study is divided into three sections. The first is for samples annealed at 1250°C or below. The second is for samples annealed at 1285°C. Finally, a batch of wafers are studied using the quick-turnaround approach.

3.1 Low-Temperature Annealed Samples

3.1.1 Experimental

The starting silicon bulk wafers were 3-5 Ω-cm Czochralski-grown wafers. An Eaton NV-200 oxygen implanter was used to implant the wafers at a substrate temperature of 500°C, using an implantation energy of 150 keV, and implant oxygen doses of 1.8 or 2.0×10^{18} cm^{-2}. Following implantation, the SIMOX wafers were annealed in an N_2/O_2 ambient at 1150°C for 3 hours or 1250°C for 2 or 16 hours. Oxygen is required in the annealing ambient in order to grow a thin oxide, to protect the Si surface from pitting. After the anneal, n-type epilayers (doped 2×10^{15} cm^{-2}) were grown to thicknesses of 1.3 to 2.0 μm. Devices were then fabricated, including laterally isolated BOXCAPs.

C-V measurements were taken at 1 MHz using an HP 4280A C-Meter. C-t measurements were obtained with the HP 4280A using an external pulse source. The C-t measurements for each interface were made by pulsing from inversion, so that the effect of the other interface could be neglected. Pulsing from inversion also minimizes the effects of interface traps on the C-t transient. Standard Zerbst analysis was used

to calculate the generation lifetime [44]. It should be noted that the films are all thick enough to avoid full depletion, and that the steady-state width of the depletion layer is always greater than the width of the original silicon seed layer. Thus, this heavily damaged region cannot be profiled, although it still contributes to the generation of minority carriers.

3.1.2. Results and Discussion

Typical C-V curves for BOXCAPs with various SIMOX process parameters are shown in Fig. 3.1. Noting that a positive bias depletes the F/O interface and a negative bias depletes the S/O interface, it is seen that the C-V curves vary with processing significantly more when the F/O interface is depleted than when the S/O interface is depleted. Thus, the F/O interface is sensitive to changes in processing. Since the minimum capacitance in inversion increases with donor density, as the oxygen dose or anneal time is increased, the film donor density increases. Lowering the anneal temperature also increases the film donor density. Fixed oxide charge rigidly shifts the C-V curves in depletion. Therefore, one can see that increasing the oxygen dose or anneal time, or lowering the anneal temperature increases Q_{fi}. Finally, since interface traps cause a stretch-out of C-V curves, it is seen that increasing the oxygen dose or lowering the anneal temperature increases D_{it1}. Therefore, the C-V measurements show that increasing the oxygen dose, the anneal time, or lowering the anneal temperature all increase the charge density at the F/O interface and increase the donor density in the film, but have little effect on the quality of the S/O interface.

In Fig. 3.2, typical C-t curves are shown for the film. The transients are very fast (< 0.3 s). A comparison of curves A and B to curves C, D, and E shows that increasing the oxygen dose or lowering the anneal temperature sharply decreases the time for the C-t transient, implying that the quality of the film near the buried oxide is degraded. This result correlates well with the results of C-V measurements, which also show that the density of defects increases with increasing dose and decreasing

anneal temperature. Furthermore, a comparison of curve A to curve B and curve C to curve D shows that longer anneals produce devices with longer C-t transients, indicating a lower defect density. This contrasts with the result of C-V analysis, which showed higher fixed oxide charge density and increased donor concentration with longer anneals. In Figure 3.3, typical C-t transients are shown for the substrate. The major trend observed in this figure is that the substrate C-t transients tend to be longer for devices with poorer quality films and buried oxides. A comparison of Figs. 3.2 and 3.3 shows that the C-t transients of the substrate are one to two orders of magnitude longer than the transients for the film, reflecting the better quality of the substrate. The higher quality of the substrate relative to the film correlates well with the results of C-V analysis, which showed the density of defects at the S/O interface to be an order of magnitude lower than at the F/O interface. Comparison of Figs. 3.2 and 3.3 also shows that the quality of the substrate changes less with processing than does the film. The relative insensitivity of the substrate to changes in processing was also found from C-V analysis when comparing the S/O and F/O interfaces. The above results plus the effects of changing the various parameters on the thickness of the buried oxide layer are tabulated in Table 3.1.

3.1.3 Discussion

Changing the dose of the implanted oxygen, the anneal temperature, and the anneal time each has certain effects on the defects of SIMOX wafers. The physical explanation of these effects are discussed as follows.

As shown above, increasing the oxygen dose results in a sharp increase in the number of electrically active defects for both the silicon film and the F/O interface. This is because increasing the oxygen dose causes more lattice damage, and produces a higher concentration of oxygen-related defects in the film. This conclusion can be seen as follows. The minority carrier generation lifetime in the film, τ_{gl} reflects the concentration of generation/recombination centers, which are dominated by bulk

midgap levels. Thus, in SIMOX material, τ_{g1} is shortened by dislocations decorated by metals and by oxygen complexes and precipitates. The film donor density, N_{d1} is increased over the nominal doping density by thermal donors (TDs) [45], which are small oxygen-containing clusters, and by "new donors" (NDs) [46], which are SiO_x precipitates. Thus, increases in donor concentration over the nominal one can be linked to increases in oxygen concentration. Since τ_{g1} is shortened and N_{d1} is increased by increasing the oxygen dose, there is a strong indication that higher doses increase the oxygen content of the top layer. Anomalous increases in donor concentration in SIMOX material have also been found by other researchers, who linked the increase to oxygen-related donors [47]. Additionally, Q_{f1} and D_{it1} increase with dose. Others have correlated increases in fixed oxide charge and interface traps to increases in the roughness of the Si/SiO_2 interface [48] (for thermally grown oxides). The increase of Q_{f1} and D_{it1} indicate that higher doses degrade the microstructure. It therefore appears that increasing the dose causes more damage and introduces more defects.

Increasing the anneal time has a mixed result. Both Q_{f1} and N_{d1} increase, indicating a degradation of the buried oxide and more oxygen activity in the film. On the other hand τ_{g1} increases, indicating a better quality film. The generation lifetime may be increased by either diffusion of metal contaminants out of the surface layer or from dissolution of the oxide precipitates. Since D_{it1} remains the same or decreases, the correct interpretation appears to be that increasing the anneal time improves the microstructure, but causes the redistribution of deep-level impurities from the film to the buried oxide. The increase in N_{d1} with anneal time may be caused by nitrogen-related complexes formed during the long anneal [47].

Increasing the anneal temperature from 1150 to 1250°C sharply improves the quality of the film and its interface with the buried oxide. Published TEM data on SIMOX wafers annealed at these two temperatures show that an 1150°C anneal leaves very high densities of dislocations and oxide precipitates, and produces a poor

F/O interface [21],[49]. Thus, it is expected that τ_{g1}, Q_{f1}, and D_{it1} reflect the poor microstructure, and with the high concentration of oxygen in the top layer, N_{d1} reflects the presence of oxygen donors.

As discussed above, changing the oxygen dose, the anneal temperature, or the anneal time has a significant effect on the quality of the film and the F/O interface. The S/O interface, however, is fairly insensitive to these process variations. Also, it is interesting that the S/O interface is much better than the F/O interface. For a dose of 1.8 or 2.0×10^{18} cm^{-2}, silicon islands exist in the buried oxide layer near the substrate, but not near the film. Thus, the islands have little effect on fixed oxide charge or interface trap densities. Although Q_{f2} and D_{it2} are comparable to thermal oxides, τ_{g2} is very low in SIMOX, as values well over 100 μs are obtained in bulk silicon. This short lifetime is most likely caused by metallic contaminants introduced during the oxygen implantation, which subsequently diffuse into the substrate during the high temperature anneal [50],[51].

For higher temperature anneals, the thickness of the buried oxide layer increases with dose, but not anneal time. The increase of thickness with dose is expected, since more oxygen is being implanted. There is no noticeable increase of oxide thickness with anneal time since the amount of oxygen precipitated out in the film and substrate is a small fraction of the amount of oxygen implanted. For a given dose, the buried oxide layer obtained after an 1150°C anneal is less than for a 1250°C anneal, showing that a significant percentage of the implanted oxygen is in the form of precipitates for the lower temperature anneal.

3.2 Samples Annealed at 1285°C

3.2.1 Experimental

N-type, 3-5 Ω-cm Si wafers were implanted with oxygen at energies and temperatures of 150 keV and 550°C, respectively. The implant doses were 1.5 or 1.8×10^{18}

cm^{-2}. Multiple implant samples with three doses of 5×10^{17} cm^{-2} were also examined. Following implantation, the wafers were annealed in an N_2/O_2 ambient at 1285°C for 2 or 6 hours. The multiple implant sample was annealed for 2 hours after each implant, to give a total anneal time of 6 hours. Three–five Ω-cm epilayers were then grown in dichlorosilane at 1050°C. Fabrication of test chips then followed. C-V and C-t measurements were then taken as described in Section 3.1.1.

3.2.2 Results and Discussion

In Table 3.2, the results of analysis of samples annealed at 1285°C are shown. Several interesting results can be seen.

First, for the low implant dose samples, an excess donor density was found. The donor density is particularly large for the single implant sample, for which ΔN_{d1} is 2×10^{16} cm^{-3}. For the multiple implant sample the excess donor concentration is smaller, but it is still 3×10^{15} cm^{-3}, which is significant when compared to the nominal doping density of 2×10^{15} cm^{-3}. The cause is the same as discussed above for samples annealed at 1150°C – oxygen-related donors. For lower oxygen doses, a smaller percentage of the implanted oxygen is incorporated into the buried oxide [10]. Thus, higher anneal temperatures are required to eliminate oxide precipitates in the film for lower implant doses. A 1285°C, 6 hour anneal is not sufficient for a 1.5×10^{18} cm^{-2} oxygen dose. This explanation is borne out in TEM photographs of the samples, which shows a high density of oxide precipitates in the Si film for both low implant dose samples (see Chap. 5).

The sample with the lowest fixed oxide charge and interface state density for the F/O interface was the standard dose (1.8×10^{18} cm^{-2}) single implant sample with the short 2 hour anneal. Relative to the LTA samples, the low dose samples have a lower Q_{fi} but a higher D_{it1}. The high interface state density is due to the interface roughness, which smears out the C-V curve. For the standard dose samples annealed for 6 hours, a surprisingly large fixed oxide charge density was seen for the

F/O interface. Since D_{it1} is reasonably low for this sample (5×10^{10} $cm^{-2}eV^{-1}$), the cause is not interface roughness. Similar results are seen for Q_{f2} and D_{it2}. A point of particular interest is the high value of D_{it2} for the low-dose single implant sample. As will be seen in Chaps. 4 and 5, upon irradiation or electric field stressing, a very large number of traps are generated at the S/O interface for this sample.

Overall, the data in Sections 3.1 and 3.2 indicates that increasing the anneal temperature reduces the defect density, increasing the anneal time increases pre-stress buried oxide defect density, and buried oxide layers formed by multiple implants have reduced defect densities.

3.3 Quick-Turnaround Studies

3.3.1 Experimental

The test structures were fabricated as follows. N-type silicon wafers of 3-5 Ω-cm were split into two lots, one of which had a 500 Å oxide grown on the front surface. The lots were implanted together with oxygen using the Eaton NV-200 oxygen implanter at IBIS Technology. The implant dose, energy and temperature were 1.8×10^{18} cm^{-2}, 150 keV and 550°C, respectively. The screen oxide was removed by sputtering during the course of implanting. Following implantation, the wafers were annealed in an N_2/O_2 ambient, at temperatures ranging from 1150 to 1285°C and for times ranging from 2 to 16 hours. Epilayers were then grown to a thickness of 1.5 μm, using dichlorosilane at 1050°C. Ohmic contacts to the front and back surfaces were formed by spinning phosphorous-doped glass on both sides of the wafers, followed by a 950°C, 15 minute drive-in. Trenches were then etched in the Si film, down to the buried oxide, forming isolated silicon islands on the buried oxide. The area of the resulting capacitors was 450×450 μm^2. Although the plasma etch used to isolate the islands may cause some sidewall damage, the sidewall area is only about 1% of the capacitor area, making its contribution to the capacitance measurements negligible. The difference between

these QT capacitors and the BOXCAPs discussed in the previous section is that the other capacitors were on a CMOS test chip, and thus experienced a large amount of post-SIMOX processing. C-V and C-t measurements were made following device fabrication.

3.3.2 Results and Discussion

Typical BOXCAP C-V curves are shown in Fig. 3.4. Although the curves shown in this figure refer to 1285°C wafers implanted with a screen oxide (SO wafers), similar trends were observed for wafers implanted without a screen oxide (NOSO wafers). Since both silicon layers are n-type, a positive bias depletes the film while a negative bias depletes the substrate. The presence of fixed oxide charge rigidly shifts the C-V curve, while interface traps cause a stretch-out, and an increase in the donor density increases the minimum capacitance. Thus, it is seen in Fig. 3.4 that the film/oxide (F/O) interface is much more sensitive to changes in the anneal parameters than is the substrate/oxide (S/O) interface. For the F/O interface, it is seen that the lower temperature anneals cause an increase in the donor density, while the longer anneals cause an increase in the fixed oxide charge density.

The analysis of the C-V and C-t data is summarized in Figs. 3.5 through 3.8. As shown in these figures, all of the parameters show improvement with anneal temperature. This effect is due to annealing out of precipitates and dislocations, as well as a sharpening of the buried oxide interfaces [19,21,47]. The increase of the film donor concentration (N_{d1}) at lower anneal temperatures has also been reported [47], and is caused by oxygen-related donors. When the anneal time is increased, τ_{g1} tends to improve, but Q_{f1} becomes higher. Surprisingly, the density of traps at the F/O interface (D_{it1}) does not increase with Q_{f1}. For thermal oxides, it has been shown that the density of both fixed oxide charge and interface traps correlates well with the roughness of the Si/SiO_2 interface [48]. This may indicate that longer anneals affect the chemistry of the oxide without making the F/O interface smoother. It is

also interesting to note that although τ_{g1} improves with anneal time, τ_{g2} is degraded by it. The increase of the film lifetime with longer anneals is probably due to a slight annealing out of the dislocations. The cause of the increase of Q_{fi} with anneal time is under further investigation. Another interesting result is that while SO wafers have longer lifetimes, NOSO wafers have a lower Q_{fi}. The interface trap densities are about the same for both wafers. It is expected that the effect of the screen oxide is to randomize the implant beam, thus reducing channeling. A reduction of channeling should make the depth profile of the as-implanted wafer tighter. However, it is difficult to extrapolate the reduced channeling to electrical effects.

The results described above correlate well with analysis of fully-processed devices [52]. In analysis of those devices, it was also found that τ_{g1} improves with anneal time while Q_{fi} increases and D_{it1} remains unchanged. Similar trends were found for changes in the anneal temperature. Although the trends are the same for the fully processed and QT material, there are differences in the actual values of the parameters. The QT material has a higher Q_{fi} and lower τ_{g1} than the fully processed devices. On the other hand, τ_{g2} is higher for the QT material. Some of the differences between the two materials may be due to the extra thermal processing of the FP devices, since this material experiences the full thermal cycling of a CMOS test chip. The only processing experienced by the QT material is the 950°C, 15 minute drive-in and the plasma trench etch. The ratio of the capacitor to sidewall area for these devices is 75 to 1. Therefore, it is unlikely that the capacitor measurements are affected by sidewall damage. To further investigate the differences between the QT and FP devices, the effect of CMOS processing was studied by giving several wafers short, low temperature anneals. This second batch of wafers was implanted in a manner similar to the first batch, without a screen oxide, and annealed at 1285°C for 6 hours. After epi growth, the wafers were annealed at 1180°C for 60 seconds, 875°C for 8 hours, 1050°C for 1 hour, or not annealed. The results of C-V measurements on these

devices are shown in Figs. 3.9 and 3.10. The x-axis is roughly in Dt (diffusivity × time) order. As can be seen, longer, higher temperature anneals reduce the defect density. Although it is known that a 1285°C, 6 hour anneal does not fully anneal out the defects in SIMOX material, it is surprising that these relatively insignificant anneals have a major impact. The 1050°C, 1 hour anneal reduces Q_{fi} by 2×10^{11} cm^{-2}. This result shows that device processing can affect the defects of the buried oxide layer.

3.4 Summary

C-V and C-t measurements have been used to analyze buried oxide layers formed by the SIMOX process. The combination of C-V and C-t measurements allows defect characterization of not only the buried oxide layer, but of its interfaces and of the silicon near the buried oxide layer. The results show that the quality of SIMOX material is enhanced by lowering the oxygen implant dose and increasing the anneal temperature, whereas increasing the anneal time improves the quality of the upper silicon layer, but lowers the quality of the film/buried oxide interface. It has also been found that the substrate/buried interface has fewer defects than the film/buried oxide interface, and that the substrate/buried oxide interface is less sensitive to changes in processing.

The QT method for fabrication of buried oxide capacitors has been shown to be a useful approach for the rapid evaluation of electrically-active defects in SIMOX wafers, particularly for process optimization. Based on analysis of wafers implanted with and without screen oxides, and annealed at various temperatures and times, it has been shown that high temperature anneals produce the best quality wafers, and that the choice of implanting with screen oxides and length of anneal time involves a trade off. The use of screen oxides and long anneals increased the generation lifetime of the Si film, but also increased the density of fixed oxide charge at the film/buried oxide interface. Finally, post-epi anneals were seen to reduce the density of fixed oxide

charge and interface traps at the film/oxide interface, showing that device processing can actually reduce the defects of the buried oxide layer.

Table 3.1. Summary of C-V and C-t Analysis on BOXCAPs. The Parameters are Defined as Follows. N_d: Donor Concentration, Q_f : Fixed Oxide Charge Density, D_{it}: Midgap Interface Trap Density, τ_g: Minority Carrier Generation Lifetime, and d: Thickness of the Buried Oxide Layer. The Numbers 1 and 2 Refer to the Film/Buried Oxide and Substrate/Buried Oxide Interfaces, Respectively.

	Dose ($\times 10^{18}$ cm^{-2}), Anneal Time (hr.)				
Parameter	1.8,3	1.8,2	1.8,16	2.0,2	2.0,16
N_{d1} ($\times 10^{15}$ cm^{-3})	19	3.2	3.5	4.5	5.1
N_{d2} ($\times 10^{15}$ cm^{-3})	2.8	2.3	2.1	2.2	1.9
Q_{f1} ($\times 10^{11}$ cm^{-2})	3.7	2.1	2.6	2.7	3.1
Q_{f2} ($\times 10^{11}$ cm^{-2})	0.3	0.1	0.15	0.15	0.2
D_{it1} ($\times 10^{11}$ cm^{-2}eV^{-1})	2.0	0.5	0.6	2.0	1.0
D_{it2} ($\times 10^{11}$ cm^{-2}eV^{-1})	<0.5	<0.5	<0.5	<0.5	<0.5
τ_{g1} (μs)	0.001	0.120	0.220	0.062	0.075
τ_{g2} (μs)	14	9	8	9	11
d (μm)	0.30	0.35	0.35	0.37	0.37

Table 3.2. Summary of C-V and C-t Analysis for samples annealed at 1285°C. The Parameters Below are Defined as Follows. N_d: Donor Concentration, Q_f : Fixed Oxide Charge Density, D_{it}: Midgap Interface Trap Density, and d: Thickness of the Buried Oxide Layer. The Numbers 1 and 2 Refer to the Film/Buried Oxide and Substrate/Buried Oxide Interfaces, Respectively.

	Dose ($\times 10^{18}$ cm^{-2}), Anneal Time (hr.)			
Parameter	0.5x3,6	1.5,6	1.8, 2	1.8,6
ΔN_{d1} ($\times 10^{15}$ cm^{-3})	20	3	0	0
Q_{f1} ($\times 10^{11}$ cm^{-2})	1.65	2.0	0.75	4.8
Q_{f2} ($\times 10^{11}$ cm^{-2})	0.2	0.6	0.3	0.9
D_{it1} ($\times 10^{11}$ cm^{-2}eV^{-1})	1.2	3.6	<0.2	0.5
D_{it2} ($\times 10^{11}$ cm^{-2}eV^{-1})	<0.2	0.8	0.3	<0.2
d (μm)	0.32	0.29	0.35	0.35

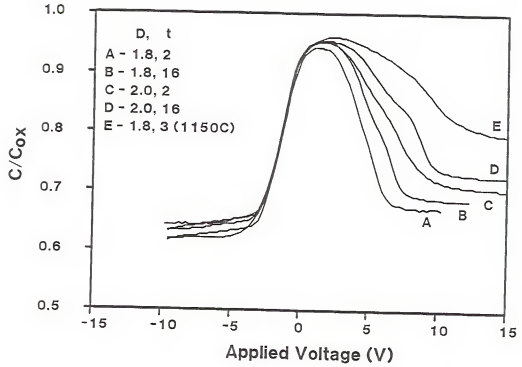


Figure 3.1. Typical high-frequency C-V curves for various oxygen implant doses, anneal temperatures, and anneal times, as indicated in the figure. The symbol "D" represents the implant dose in units of 10^{18} cm^{-2}, and "t" represents the anneal time in hours.

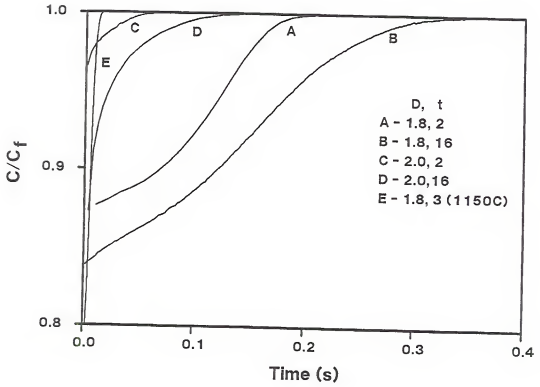


Figure 3.2. Typical C-t transients (normalized with respect to the final capacitance) for various oxygen implant doses, anneal temperatures, and anneal times, as indicated in the figure, when epilayer is pulsed into strong inversion. The symbol "D" represents the implant dose in units of 10^{18} cm^{-2}, and "t" represents the anneal time in hours. Results are shown for the film.

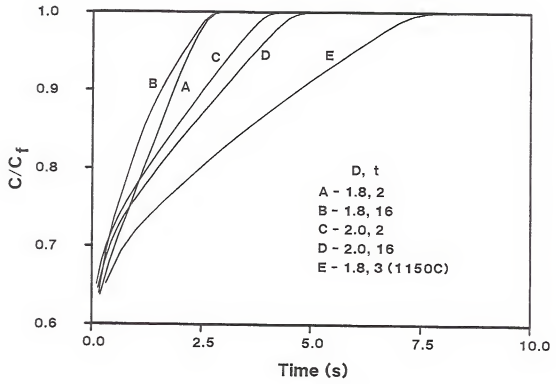


Figure 3.3. Typical C-t transients (normalized with respect to the final capacitance) for various oxygen implant doses, anneal temperatures, and anneal times, as indicated in the figure, when epilayer is pulsed into strong inversion. The symbol "D" represents the implant dose in units of 10^{18} cm^{-2}, and "t" represents the anneal time in hours. Results are shown for the substrate.

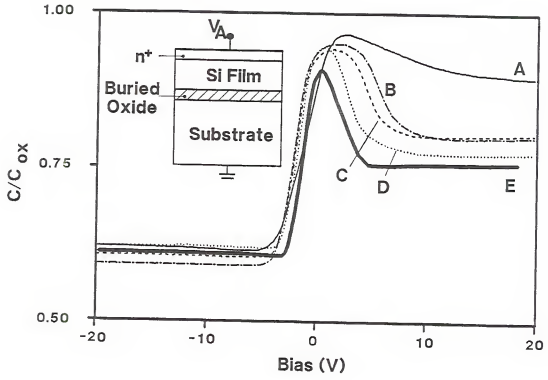


Figure 3.4. Typical C-V curves for SIMOX buried oxide capacitors with various anneals. The curves are for wafers implanted with a screen oxide. Curve A represents material annealed at 1250°C for 2 hours, curve E is an ideal curve, and curves B, C, and D represent material annealed at 1285°C for 16, 8 and 2 hours, respectively.

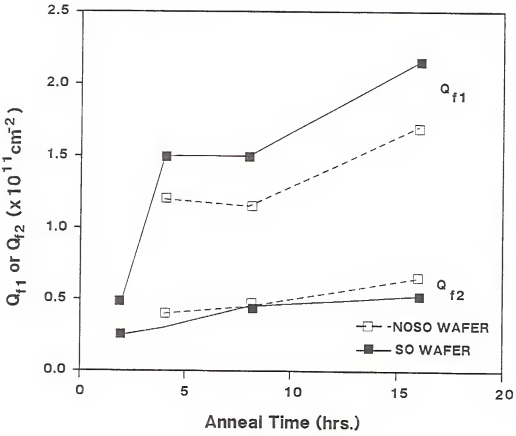


Figure 3.5. The change in fixed oxide charge density at both the film/oxide interface and the substrate/oxide interface. A comparison between wafers implanted with and without screen oxides is also shown.

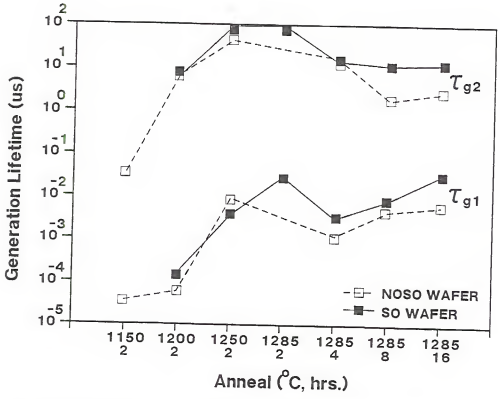


Figure 3.6. The effect of changing both the anneal temperature and anneal time on the film and substrate minority carrier generation lifetimes, for wafers inplanted with and without screen oxides. On the x-axis labels, the top numbers are the anneal temperatures while the bottom numbers are the anneal times.

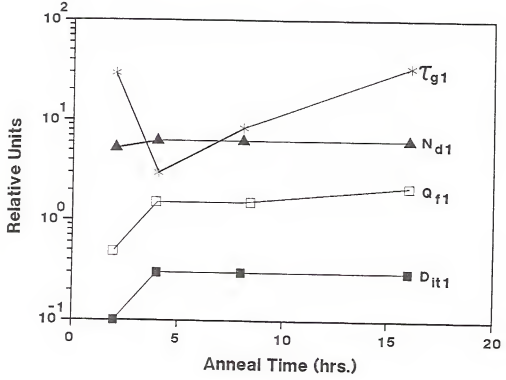


Figure 3.7. Summary of the effect of changing the anneal time on the various parameters of the film and the film/oxide interface. Results are shown for wafers implanted with a screen oxide and annealed at 1285°C. The unit of τ_{g1} is μs, N_{d1} is 10^{15} cm^{-3}. Q_{f1} is 10^{11} cm^{-2}, and D_{it1} is in 10^{11} eV^{-1}cm^{-2}.

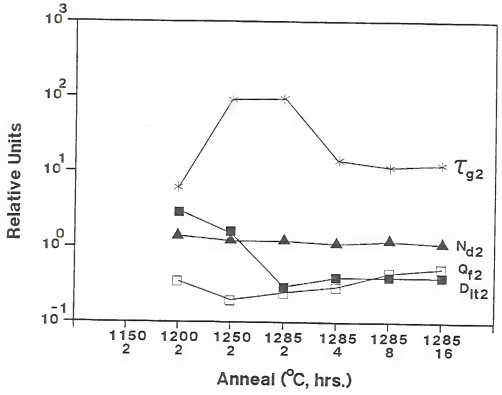


Figure 3.8. Summary of the effect of changing the anneal time on the various parameters of the substrate and the substrate/oxide interface. Results are shown for wafers implanted with a screen oxide and annealed at 1285°C. The unit of τ_{g1} is μs. N_{d1} is 10^{15} cm^{-3}, Q_{f1} is 10^{11} cm^{-2}, and D_{it1} is in 10^{11} eV^{-1}cm^{-2}.

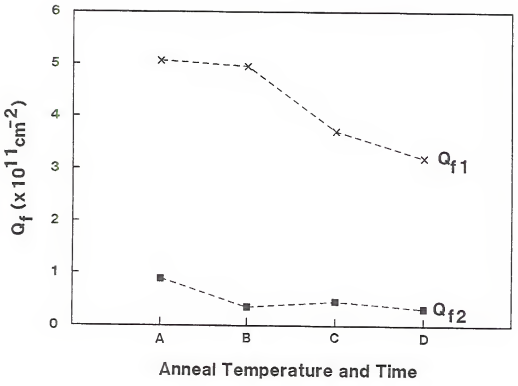


Figure 3.9. The effect of various low temperature anneals on the fixed oxide charge density. On the x-axis, 'A' represents samples with no anneal, 'B' represents samples annealed at 1180°C for 60 s, 'C' represents samples annealed at 875°C for 8 hours, and 'D' represents samples annealed at 1050°C for 1 hour.

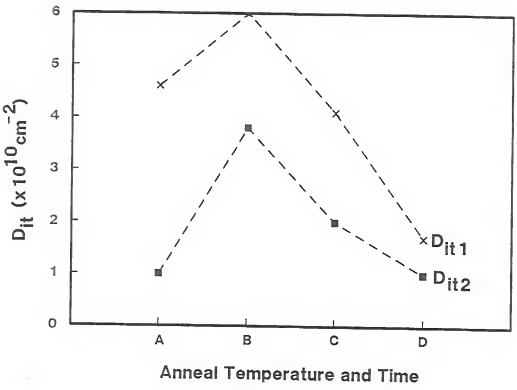


Figure 3.10. The effect of various low temperature anneals on the interface state density. On the x-axis, 'A' represents samples with no anneal, 'B' represents samples annealed at 1180°C for 60 s, 'C' represents samples annealed at 875°C for 8 hours, and 'D' represents samples annealed at 1050°C for 1 hour.

CHAPTER 4
THE EFFECTS OF TOTAL DOSE IRRADIATION ON THE CHARGE TRAPPING OF THE BURIED OXIDE LAYER

Much of the interest in SOI technology is based on the enhanced immunity of SOI circuits to transient radiation and single event upset [53]–[62]. However, the buried oxide layer presents an additional oxide whose response to total dose irradiation must be characterized. This is especially true for buried oxide layers formed by the SIMOX technique. Clearly, the SIMOX process is much different from the conventional thermal and CVD oxides. Depending on the post-implant anneal, one can have a highly defective structure (such as oxide precipitates in the Si film, silicon precipitates in the oxide, and oxide protrusions into the Si film) or a high quality structure with very sharp oxide interfaces and few defects in the Si film. The effect of processing on SIMOX material, devices, and circuits has been well documented [8]–[32]. However, few studies have been published on the effects of total-dose irradiation on SIMOX buried oxides, particularly in relation with SIMOX processing. In addition, most groups investigating total dose effects have studied the buried oxide charge trapping by measuring the leakage or threshold voltage shifts of the backchannel transistor. Therefore, one of the objectives of this work has been to investigate the effects of changing the various SIMOX process parameters on the charge trapping of the buried oxide layer. The buried oxide characteristics are studied directly by high-frequency C-V measurements. The effects of varying the implant oxygen dose, and the post-implant anneal temperature and time are studied. In addition, the post-irradiation charge trapping is correlated to the pre-radiation charge densities. A major result is that a large increase in the film donor density with X-ray dose is seen for low oxygen dose samples.

4.1 The Interaction Between Ionizing Radiation and the Si/SiO_2 System

4.1.1 Radiation Generated Damage

Ionizing radiation (e.g. X-rays, gamma rays, high energy electrons) can interact with a semiconductor in either of two ways. If the energy of the radiation is sufficient, it can knock an atom out of its place in the lattice. Radiation also breaks the bonds between neighboring atoms, generating electron-hole (e-h) pairs. The effects of lattice damage and bond-breaking on the performance of devices can be divided into two categories: transient effects and total dose effects. Transient effects concern the effects of the generated excess electron-hole pairs. The sudden surge of excess carriers can turn on parasitic bipolar transistors and thyristors. This action can upset logic states or even burn out the device. Total dose effects include the gradual build up of lattice damage and trapped electron and holes as the device is irradiated. In bipolar transistors, the lattice damage lowers the minority carrier lifetime, thus decreasing the transistor gain. In addition, the generated carriers can be trapped at the surface of the transistor, turning on p-n junctions in a manner similar to gated diodes. MOS devices, being majority carrier devices, are relatively insensitive to lattice damage. However, they are sensitive to transient effects and to broken bonds in the oxide and at the oxide/silicon interface. Since the topic of this chapter is total dose effects, the remainder of this section will concern charge trapping in the oxide.

4.1.2 Radiation Generated Defects in MOS Structures

The details of the dynamics of the formation and annealing of radiation defects in SiO_2 are very complicated. The exact sequence of the device processing is very important. However, the basic mechanisms are as follows.

When ionizing radiation passes into an oxide, the incident energy creates electron-hole pairs along its track. It has been shown that one e-h pair is created per 18 eV [63]. Immediately after generation, some of the e-h pairs recombine. The percentage of e-h pairs recombining depends the applied field and the energy of the particle. The

recombination rate is higher for lower electric fields and particles that create dense tracks. At room temperature, electrons have a fairly high mobility in SiO_2 (about 20 $cm^2V^{-1}s^{-1}$) [64]. Most oxides have few electron traps, so that the excess electrons are swept out of the oxide on a time on the order of the dielectric relaxation time (picoseconds). The transport of holes, rather than being characterized by a single mobility, is characterized by a very slow, dispersive hopping transport. The averaged mobility of the holes is below 10^{-4} $cm^2V^{-1}s^{-1}$ [65]. In addition to the dispersive transport, a high density of hole traps are found near and at the oxide interfaces. The trap density is a very sensitive function of processing. The mechanism for the formation of interface states is still somewhat controversial, but the existence of a two step process is essentially agreed upon. In the first step, holes drifting through the oxide react with hydrogen to generate H^+. In the second step, the hydrogen ion drifts to the interface, where it reacts with hydrogen already present to produce H_2 plus a dangling silicon bond. The dangling silicon bond is the amphoteric P_b center. The main controversy is whether the protons are generated near the interface [66] or in the bulk of the oxide [67]. The interaction of radiation and SIMOX buried oxides is sketched in an energy band diagram in Fig. 4.1.

4.2 Experimental Details

N-type, 3 – 5 Ω-cm silicon wafers were implanted with oxygen, with implant doses ranging from 1.5 to 2.0×10^{18} cm^{-2}. Following the oxygen implant, the wafers were annealed at either 1250 or 1285°C in an N_2/O_2 ambient, for 2, 6, or 16 hours. Some multiple implant wafers were also examined. The multiple implant was carried out by performing three implants of 5×10^{17} cm^{-2}. Each implant was followed by a 2 hour anneal at 1285°C for 2 hours, giving a total anneal time of 6 hours. Following the SIMOX processing, 3 – 5 Ω-cm n-type epilayers were grown in dichlorosilane at 1050°C. The net Si film thickness was around 1.5 μm. Devices were then fabricated, including buried oxide capacitors (the capacitor formed between the film and

substrate with the buried oxide as the capacitor dielectric) and backgate transistors. The unlidded devices were irradiated with 10 keV X-rays using an Aracor 4100 Semiconductor Irradiation System. Irradiation was performed with all contacts to the film grounded, and a 0 or -5 V bias applied to the substrate. Threshold voltage and subthreshold slope measurements were taken immediately following irradiation, followed by high-frequency (1 MHz) C-V measurements on the BOXCAPs (Buried OXide CAPacitors).

4.3 Basic Radiation Response

4.3.1 Results

In the following discussion, all voltage shifts referred to are given by their absolute values. In Fig. 4.2, the effect of increasing the X-ray dose on the back-channel transistors and on the buried oxide capacitor is shown, for the case of a grounded substrate. The midgap voltage, V_{mid}, is defined as the voltage for which the Fermi level at the Si/SiO_2 interface is in the middle of the bandgap. Although both donor and acceptor type traps are found in both halves of the bandgap [68,69], the neutral point is only a few kT/q from midgap [69] (for ionizing radiation). Thus, ΔV_{mid} is a good approximation of the voltage shift due solely to oxide charge. This quantity is calculated from the shifts in the BOXCAP C-V curves. The threshold voltage for MOSFETs (V_t), on the other hand, is related to the sum of oxide charge and interface traps at the energy level corresponding to the onset of inversion. Since a good correlation is seen between ΔV_{mid} and ΔV_t, few interface traps are being created. The effect of a negative substrate bias during irradiation can be seen in Fig. 4.3. As can be seen, a negative bias reduces the trapping of holes at the F/O interface , especially at doses above 100 kRad. The curves for ΔV_{mid1} and $\Delta V_{tn,p}$ are essentially parallel, showing that very few interface states are generated, even at 1 Mrad. This result can be seen more specifically in Fig. 4.4, in which the subthreshold slope and interface face trap density are both plotted versus dose. Even at a dose

of 1 Mrad, the subthreshold slopes are close to their pre-irradiation values and the density of midgap interface traps that has been generated is only 1×10^{11} $eV^{-1}cm^{-2}$. The effects of total X-ray dose and substrate bias are shown in detail in Figs. 4.5 and 4.6. In these figures, The degradation of the subthreshold slope is shown for both n- and p-channel devices. BOXCAP data is not shown, because the C-V curves were shifted beyond the voltage range of the C-V meter for the biases at which the generated interface trap density became important. It is seen that ΔD_{it1} is negligible except for positive biases and for X-ray doses greater than 100 krad. The average interface state density can be estimated from the subthreshold slope measurements by [70]

$$\Delta D_{it} = \frac{C_{ox}\Delta S}{kTln(10)} \tag{32}$$

where ΔS is the change in the subthreshold slope, and the other variables have their usual meanings. Using the above equation, it is estimated that 2.4×10^{11} $eV^{-1}cm^{-2}$ traps are generated at 500 krad with a substrate bias of 5 V. The number of generated traps is below 1×10^{11} except for a total dose above 50 krad and a 5 V substrate bias.

Next, the effect of bias on the charge trapping at the two BOX interfaces is examined. In Fig. 4.7, the density of trapped charge at both interfaces is shown as a function of dose for substrate biases of 0 and -5 V. For a 0 V bias, the roughly equal densities of charge are trapped at both oxide interfaces. For a -5 V bias, however, the trapping of holes at the S/O (substrate/oxide) interface is greatly enhanced, even at a dose of 10 kRad. At the F/O (film/oxide) interface, the -5 V bias keeps the increase of trapped charge with dose relatively flat. Previous work on the total dose response of buried oxide layers has indicated that there is a bias region for which the trapping of charge is minimized. In order to investigate this effect, Q_{ot1} as well as $\Delta V_{tn,p}$ are plotted as a function of substrate bias and X-ray dose in Figs 4.8 – 4.10. In each of these graphs, it is seen that the substrate bias required to minimize the

charge trapping becomes more negative with total dose. The minimum exists from competition between three effects. The first is that as the field in the oxide increases, a higher percentage of electron-holes pairs escape geminate recombination. Thus, more holes survive to be trapped at the interface. The second effect is that as an increasingly negative bias is applied to the substrate, holes are repelled from the F/O interface. The third effect is that the capture cross section decreases as the electric field in the oxide increases.

4.3.2 Discussion

The pre-radiation density of electrically-active defects is much higher in the film and at the F/O interface than in the substrate and at the S/O interface [52],[71]. To see how this affects the post-radiation charge trapping characteristics, we plot both Q_{ot1} and Q_{ot2} versus the substrate bias in Fig. 4.11. For a bias of 0 V or one that attracts holes to the interface, the F/O interface traps slightly fewer holes than the S/O interface. It is interesting that although $Q_{f1} > Q_{f2}$, $Q_{ot1} < Q_{ot2}$. For an attractive bias, the rate of charge build is 3.80×10^{11} cm^{-2}/V at the F/O interface and 3.86×10^{11} cm^{-2}/V for the S/O interface. This implies that despite the higher density of fixed oxide charge and interface traps at the F/O interface, the number of hole traps is nearly the same at both interfaces. However, when holes are being repelled from the interface under consideration, the S/O interface traps less holes, as seen by the fact that the minimum Q_{ot} is lower for the S/O interface than for the F/O interface. Since silicon islands are found in the buried oxide layer near the S/O interface, but not near the F/O interface, it is expected that the S/O interface would have more traps than the F/O interface. An alternative explanation may be that holes are trapped throughout the bulk of the oxide, rather than at the interfaces. Using photoyield experiments, workers at Harry Diamond Labs found that holes were trapped in place almost immediately following generation [72,73]. This could account for the similarity in the charge trapping as determined by the voltage shifts at the

oxide interfaces. The low density of generated interface traps can also be explained by the lack of hole movement. As discussed above, the generally accepted models of interface trap generation all require that H^+ be generated by hole transport.

An additional comment should be made on the use of negative substrate biases during irradiation. Clearly, the total dose hardness of the buried oxide is greatly improved by the use of a negative bias. Since the voltage shifts for a zero volt substrate bias are significant, a negative bias is needed to reduce the backchannel voltage shift to keep the circuits functional. Thus, technically, the negative bias is clearly beneficial. However, from the perspective of a systems designer, the need for an additional supply and/or pin compatibility can be major issues, and a circuit requiring a negative bias may not be acceptable.

4.4 The Effects of Processing

The SIMOX process parameters investigated in this study were the dose of the oxygen implant, the temperature of the post-implant anneal, and the time of the post-implant anneal. Of these parameters, charge trapping at the F/O interface appeared to be most sensitive to the post-implant anneal parameters. Although the dose of the oxygen implant has little effect on the F/O interface charge trapping, low oxygen dose material exhibits an increase in the film donor density with X-ray dose. A similar, but weaker, process dependence was seen for charge trapping at the S/O interface. An exception to this is the low dose single implant material, for which large increases in ΔD_{it2} and Q_{ot2} were found. For both interfaces, a trend is seen towards reduced charge trapping for samples with lower initial charge densities. Since similar results were obtained for ΔV_{tp} and ΔV_{tn}, the following discussion will focus on ΔV_{tp} only.

4.4.1 The Film/Buried Oxide Interface

The effects of varying the implant dose and anneal time are shown in Figs. 4.12 and 4.13, for samples annealed at 1250°C and irradiated with $V_{sub} = 0$ V. Since the

thickness of the buried oxide, hence the number of electron-hole pairs generated in the oxide, increases with the oxygen dose, so should the charge trapping (ideally). However, it is seen that the implant dose has little effect on the density of trapped charge at the film/buried oxide interface (Q_{ot1}). Note that the voltage shifts corresponding to these charge densities are greater for the higher dose samples, since $V_{ot} = Q_{ot}d_{ox}/\epsilon_{ox}$. This seen in Fig. 4.13, where ΔV_{tp} is shown as a function of X-ray dose. Increasing the anneal time from 2 to 16 hours, however, strongly reduces Q_{ot1}. The reduction is by around 5.5×10^{11} cm^{-2}. As discussed above, irradiating with a negative bias reduces the charge trapping. From Figs. 4.14 and 4.15, it can be seen that the relative reduction is essentially the same for the various samples, showing that the negative bias does not change the effect of processing on the charge trapping of the BOX.

The trapped charge density is also greatly reduced when the anneal temperature is increased. A comparison of Figs. 4.12 and 4.16 shows that for samples with an implant dose of 1.8×10^{18} cm^{-2} and annealed for 2 hours, Q_{ot1} is reduced by 6.5×10^{11} cm^{-2}. As with samples annealed at 1250°C, changing the oxygen dose has little effect on the charge trapping for samples annealed at 1285°C. However, for this anneal temperature, increasing the anneal time has little effect over most of the X-ray dose range. The anneal time range is smaller for the samples in the 1285°C group than in the 1250°C, but the trend is still clear. In thermal oxides, ion implantation typically causes electron traps, which can enhance the radiation hardness by compensating the hole traps [74]. However, in SIMOX materials, our data indicates that the oxygen implant damage creates more hole traps than electron traps, since annealing reduces the net positive charge.

It was previously reported that total dose irradiation generates few interface trap in SIMOX buried oxides [75]. However, in this study, significant interface trap generation at both buried oxide interfaces was found for samples implanted with an

oxygen dose of 1.5 or 1.8×10^{18} cm^{-2} and annealed at 1285°C for 6 hours. The density of traps at the F/O interface is graphed in Fig. 4.17. It is interesting that both of these samples show large increases in ΔD_{it} and Q_{ot} at higher X-ray doses.

In addition to increasing the charge densities of the buried oxide layer, for certain samples, total dose irradiation was found to increase the effective donor density in the film. For the low (1.5×10^{18} cm^{-2}) implant dose samples, a large (4 to 8 $\times$ 10^{16} cm^{-3} at 1 Mrad) increase in the donor density was seen following irradiation. This can be seen in the C-V curves, shown in Figs. 4.18 – 4.20. Both the film and substrate in these samples are n-type, and the C-V curves were taken with the substrate grounded. Thus, the positive bias portion of the curves corresponds to depletion of the F/O interface while the negative bias portion corresponds to depletion of the S/O interface. For the low implant dose samples, the minimum capacitance of the F/O interface increases with X-ray dose. There are several effects that can change this capacitance, including non-negligible capacitances of interface traps or minority carriers, a leaky oxide, an oxide whose effective capacitance changes, or an increase in the film donor density. Capacitance measurements as a function of frequency showed that the minimum capacitance was frequency-independent above 100 kHz, proving that minority carriers and interface traps do not contribute to the measured capacitance. The fact that "good" C-V curves were obtained shows that the capacitor was not leaky. Finally, Since the minimum capacitance of the S/O interface does not change (excluding the sample with a high ΔD_{it2}), one can be sure that the oxide capacitance is constant throughout the irradiation. This leaves an increase in the donor density as the cause for the capacitance increase. In Fig. 4.21, the increase in the film density (ΔN_{d1}) is shown as a function of irradiation dose. The donor enhancement (DE) effect was also seen for material with an implant dose of 2.0×10^{18} and annealed at 1250°C for 2 hours, but it was fairly small. Note that the multiple implant samples exhibit a much stronger DE effect than the single implant

samples. Furthermore, the magnitude of the DE effect was found to be independent of the substrate bias during irradiation. We next discuss the source of the DE effect.

It is widely known that in bulk silicon oxygen complexes and SiO_x precipitates can act as donor centers [45],[46] (known as thermal donors and new donors, respectively). Furthermore, it has been shown that thermal donors (TDs) and new donors (NDs) can be active in SIMOX material annealed at temperatures below 1300°C [47]. It is also known that as one lowers the implant dose, for a given anneal, more oxygen remains in the Si film. In the low implant dose samples in this study, a high pre-irradiation film donor density was found (see Section 3.2). We therefore believe that either TDs or NDs are responsible for the DE effect. To support this thesis, TEMs were performed on the low dose samples and on a higher dose samples which did not exhibit the DE effect (see Chap. 5). The multiple implant material was found to have a very high density of precipitates near the buried oxide. The low dose single implant material was seen to have a high density of precipitates, but not as high as the multiple implant sample. Very few precipitates were seen for the material with the 1.8×10^{18} cm^{-2} implant dose. Thus, the amount of precipitates correlates well with the DE effect. Also, note that the DE effect has not been observed for the substrate, and precipitates were not observed in the substrate for any of the samples. Thus, we believe that the DE effect is related to radiation-induced states at the precipitate/film interfaces. Note, however, that the precipitate density does not correlate well with the pre-rad donor effect. The pre-rad effect may be due to TDs.

It is important to consider how the DE effect may affect the performance of irradiated devices. For example, the addition of donors will compensate the body of the n-channel devices, thus reducing the backchannel threshold voltage and increasing the backchannel leakage. In p-channel devices, the well doping near the buried oxide will increase, thus increasing the drain junction leakage.

A discussion of the effect of processing on the radiation response is incomplete

without correlating it to the pre-rad defect densities. In previous publications, we showed that Q_{fl} increases with oxygen dose and anneal time, and decreases with higher anneal temperatures [71],[76]. The trap density at the F/O interface was found to increase with oxygen dose, decrease with higher anneal temperatures, and to be insensitive to the anneal time. The general trends seen for the sensitivity of the F/O interface to SIMOX processing are summarized in Table 4.1. The lowest overall charge density is obtained for SIMOX material with a low oxygen dose and a higher post-implant anneal temperature. Increasing the anneal time improves Q_{ot1} but increases Q_{fl}. The reduction of the net positive charge with anneal time may be related to the anneal procedure. It has been reported that long anneals in an N_2 ambient can cause a nitrogenization of the F/O interface [77]. Oxynitrides have electron traps that partially compensate the hole traps. This could explain the reduction of Q_{ot1} with anneal time. The data in Table 4.1 indicates a rough correlation of the pre- and post-rad charge densities. To investigate this, Q_{ot1} is plotted versus Q_{fl} for a total dose of 1 Mrad in Fig. 4.23. Although the plot is somewhat scattered, a rough trend is seen towards reduced charge trapping in samples with a low initial fixed oxide charge density. For samples irradiated with a -5 V substrate bias, the trend is weaker, showing that a substrate bias reduces the effects of processing, and that some minimum intrinsic trapping limit is reached. It is also seen that irradiating with a -5 bias typically reduces Q_{ot1} by 5×10^{11} cm^{-2}. Extrapolating the $V_{sub} = 0$ V data to $Q_{fl} = 0$ indicates that the minimum charge trapping that can be expected is still above 5×10^{11} cm^{-2}. To achieve greater hardness, one must either apply a negative bias or greatly reduce the buried oxide thickness.

4.4.2 The Substrate/Buried Oxide Interface

The effects of varying the SIMOX processing variables on charge trapping at the substrate/buried oxide (S/O) interface can be seen in Figs. 4.24 and 4.25. For material annealed at 1250°C, Q_{ot2} is nearly independent of processing. This contrasts

with Q_{ot1}, which was found to be sensitive to the anneal time. Samples annealed at 1285°C were also found to have a Q_{ot2} relatively independent of processing. An exception to this is the single-implant low oxygen dose sample, which exhibited high trapped charge and interface trap densities. The reason for the relative insensitivity of Q_{ot2} to processing is that the S/O interface itself changes very little with processing. As discussed below, this correlates well with our pre-rad studies, which show that Q_{f2} is also relatively insensitive to processing changes. The reason for the high Q_{ot2} for the low dose single implant is can be found by examining TEM photos. TEMs show a that the S/O interface is rough, and a very high density of islands is seen in the buried oxide. This most likely leads to a high density of dangling or easily broken bonds, which then act as traps.

A comparison of Figs. 4.12 and 4.24 and 4.13 and 4.25 shows that Q_{ot1} and Q_{ot2} tend to have nearly identical functional dependencies on the total X-ray dose (for irradiation with the substrate grounded). At higher total doses, Q_{ot2} always increases a little faster. This result is very consistent for a large number of wafers. This result has practical applications for ultra thin SIMOX wafers, in which the Si film is too thin for buried oxide capacitor analysis of the film. In this material, one could extrapolate charge trapping at the F/O interface from the Q_{ot2} measured by C-V analysis of the S/O interface.

For the S/O interface, few interface traps were found to be generated. However, as seen for the F/O interface, the single implant samples annealed for six hours were found to have high densities of interface traps generated. For the standard dose material, ΔD_{it1} is less than ΔD_{it2}, by around 2×10^{11} $eV^{-1}cm^{-2}$. For the low dose sample, ΔD_{it2} is very high, as seen in Fig. 4.20. At low X-ray doses, a stretchout of the C-V curve is seen when the S/O interface is near inversion. As the total dose increases, the magnitude of the stretchout increases, and begins around midgap. Finally, at high X-ray doses, the stretchout begins when the interface is in

weak accumulation, and the trap density is so high that the Fermi level is essentially pinned.

To compare the pre- and post-irradiation charges of the S/O interface, Q_{ot2} is plotted versus Q_{f2} in Fig. 4.26. Although some scatter is seen in the data, Q_{ot2} is seen to increase with Q_{f2}. This correlates well with a similar plot for the F/O interface in Fig. 4.23. An interesting difference between the two interfaces is that while $Q_{f2} << Q_{f1}$, $Q_{ot1} < Q_{ot2}$. This may be related to the presence of Si islands in the buried oxide. The islands are predominantly found near the S/O interface. Hole traps may be associated with the interface between these islands and the oxide.

4.5. Summary

High-frequency C-V analysis and backchannel transistor measurements have been used to study the effects of total dose X-ray irradiation on the oxide charge and interface state densities at the silicon/buried oxide interfaces. The buried oxide layers were found to have a very low rate of interface trap generation. A negative bias was found to reduce the buildup of charge at the film/oxide interface, and a bias region was found for which charge trapping was minimized. A comparison of the radiation response of the two buried oxide interfaces revealed that for a 0 V substrate bias, or one that attracts holes to the interface, the film/oxide interface has less charge build up, while a for a substrate bias that repels holes from the interface, the substrate/oxide interface has less charge build up.

SIMOX buried oxides with various oxygen doses and post-implant anneal temperatures and times were irradiated with X-rays to investigate the effect of SIMOX processing on the total dose hardness on the buried oxide layer. Charge trapping at the substrate/buried oxide interface was found be fairly independent of processing. For the film/buried oxide interface, the charge trapping of samples annealed at 1250°C was reduced by long anneals. Samples annealed at 1285°C, however, were

found to be insensitive to the anneal time. At both anneal temperatures, the dose of the oxygen implant did not have a major impact on the charge trapping in the buried oxide. The results indicate a trend towards reduced charge trapping for samples with lower pre-rad fixed oxide charge. However, the it appears that the post-rad charge density (for irradiation with the substrate grounded) saturates above 5×10^{11} cm^{-2}. Thus, additional measures are needed to reduce the voltage shift at the film/oxide interface.

Although the implant dose had only a small effect on the buried oxide charge trapping, samples implanted with an oxygen dose of 1.5×10^{18} cm^{-2} exhibited a large increase in the film donor density with X-ray dose. This donor enhancement effect correlates well with the presence of oxygen precipitates in the film. The DE effect is important since the donors can compensate the back channel doping in n-channel devices, increasing the leakage.

Table 4.1. Changes in the pre- and post-irradiation charge densities of the F/O interface as the implant dose (O_2 Dose), anneal temperature (T_A), and anneal time (t_A) are increased. A dash indicates no change in the parameter.

Parameter	O_2 Dose	T_A	t_A
Q_{fl}	↑	↓	↑
Q_{otl}	-	↓	↓
D_{itl}	↑	↓	-
ΔD_{itl}	-	-	-

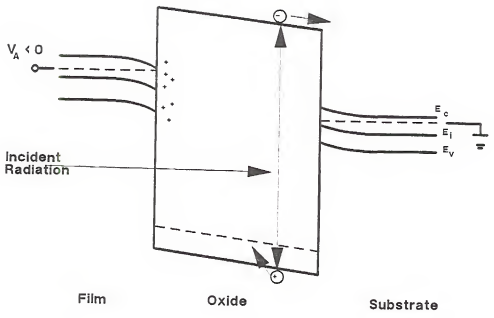


Figure 4.1. Energy band diagram, showing the generation of electon-hole pairs by ionizing radiation.

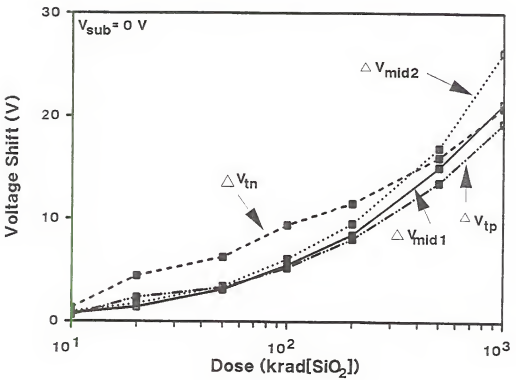


Figure 4.2. Magnitude of voltage shift versus x-ray dose for the buried oxide capacitor and for n- and p-backchannel transistors, for the case of the substrate grounded during irradiation. $\Delta V_{tn,tp}$ represents the threshold voltage of the n and p-channel transistors, while $\Delta V_{mid1,mid2}$ represents the midgap voltage shift at the film/oxide and substrate/oxide interfaces, respectively.

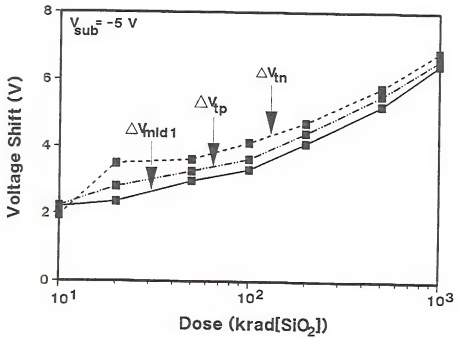


Figure 4.3. Magnitude of voltage shift versus x-ray dose for the buried oxide capacitor and for n- and p-backchannel transistors, for the case of a -5 V substrate bias during irradiation. $\Delta V_{tn,tp}$ represents the threshold voltage of the n and p-channel transistors, while ΔV_{mid1} represents the midgap voltage shift at the film/oxide and substrate/oxide interfaces, respectively.

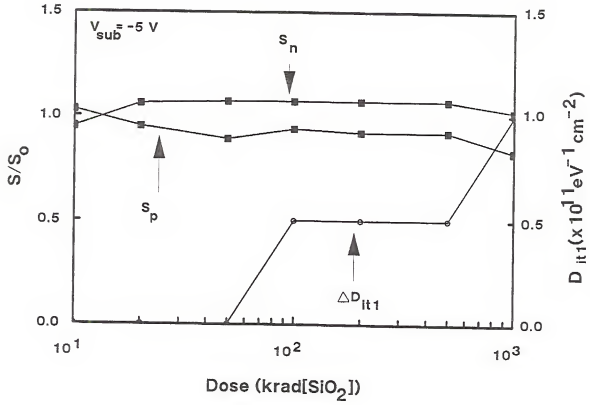


Figure 4.4. Degradation of the subthreshold slope for the n- and p-channel backgate transistors and generation of midgap interface traps as a function of dose. The quantities S_n and S_p represent changes in the subthreshold slopes of the n- and p-backchannel transistors, while D_{it1} represents the density of interface traps generated at the film/oxide interface. A bias of -5 V was applied during irradiation.

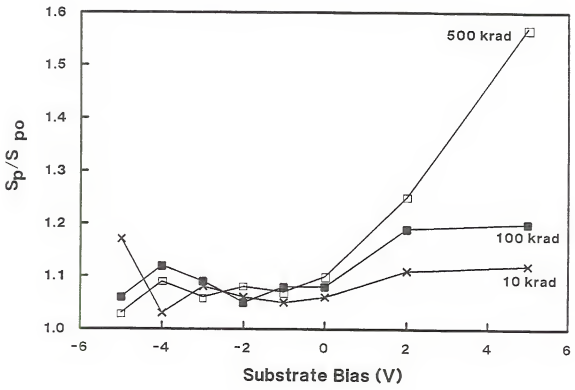


Figure 4.5. Degradation of the backchannel subthreshold slope for p-channel devices, as a function of X-ray dose and substrate bias.

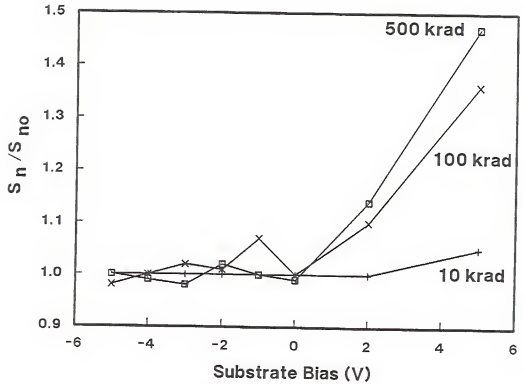


Figure 4.6. Degradation of the backchannel subthreshold slope for n-channel devices, as a function of X-ray dose and substrate bias.

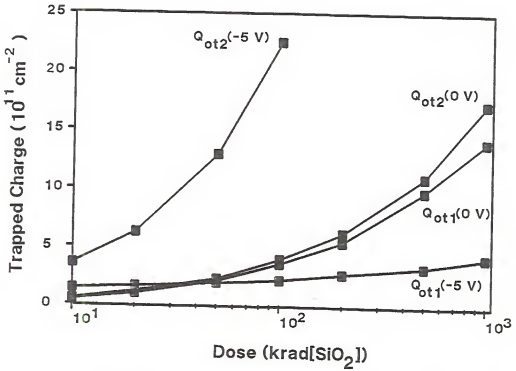


Figure 4.7. Comparison of trapped charge at both buried oxide interfaces for the cases of 0 and -5 V substrate bias during irradiation. The subscripts "1" and "2" refer to the film/oxide and substrate/oxide interfaces, respectively.

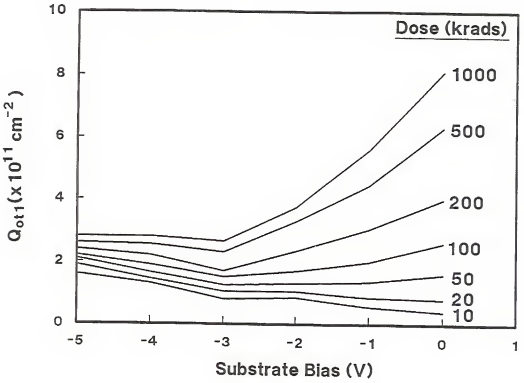


Figure 4.8. Charge trapping at the film buried oxide interface, as a function of X-ray dose and substrate bias.

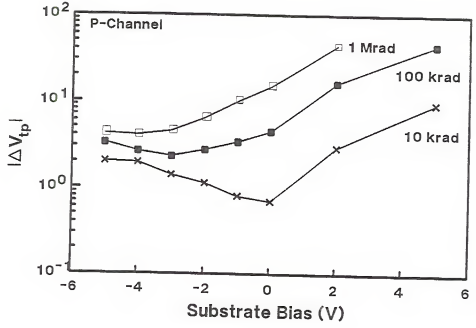


Figure 4.9. The magnitude of the p-backchannel threshold voltage shifts as a function of X-ray dose and substrate bias.

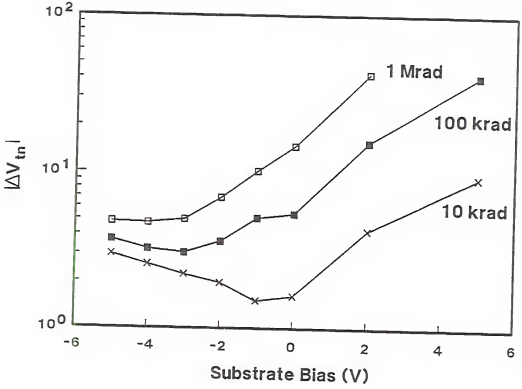


Figure 4.10. The magnitude of the n-backchannel threshold voltage shifts as a function of X-ray dose and substrate bias.

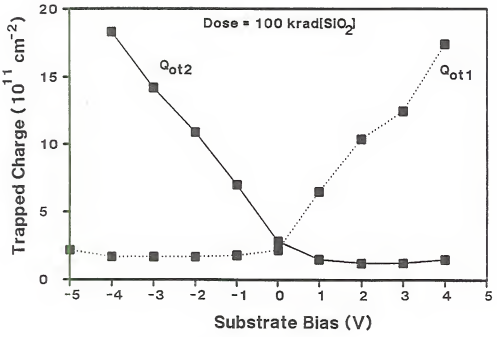


Figure 4.11. Effect of substrate bias on trapping of charge at the film/oxide and substrate/oxide interfaces, for a dose of 100 kRad(SiO_2). The quantities Q_{ot1} and Q_{ot2} refer to the film/oxide and substrate/oxide interfaces, respectively.

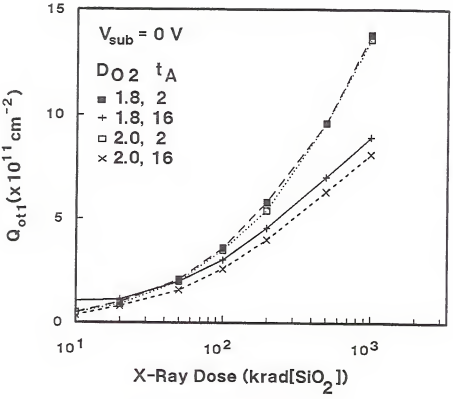


Figure 4.12. The total dose charge trapping for samples annealed at 1250°C, for irradiation with the substrate grounded. The oxygen dose (10^{18} cm^{-2}) and anneal time (Hr.) are given for each material in the legend.

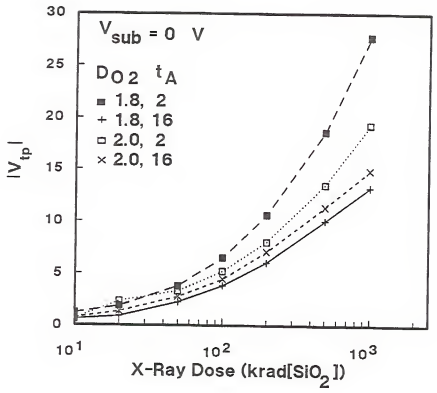


Figure 4.13. The p-channel threshold voltage shift for samples annealed at 1250°C, for irradiation with the substrate grounded. The oxygen dose (10^{18} cm^{-2}) and anneal time (Hr.) are given for each material in the legend.

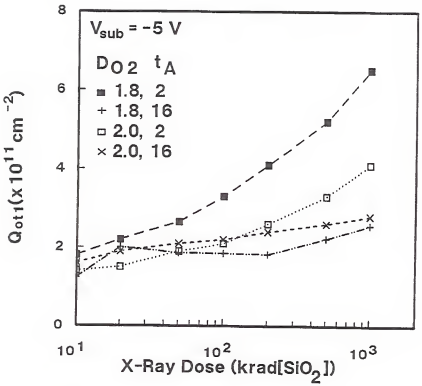


Figure 4.14. The total dose charge trapping for samples annealed at 1250°C, and irradiated with a -5 V substrate bias. The oxygen dose (10^{18} cm^{-2}) and anneal time (Hr.) are given for each material in the legend.

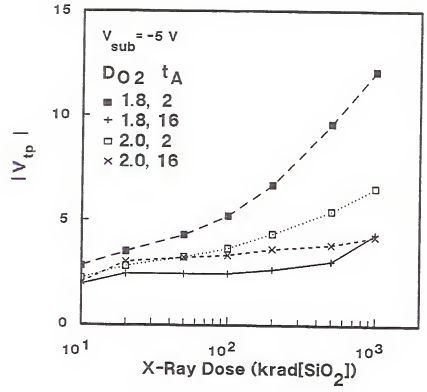


Figure 4.15. The p-channel threshold voltage shift for samples annealed at 1250°C, and irradiated with a -5 V substrate bias. The oxygen dose (10^{18} cm^{-2}) and anneal time (Hr.) are given for each material in the legend.

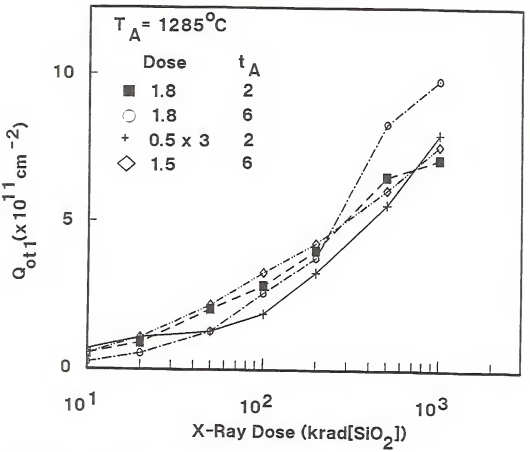


Figure 4.16. Charge trapping at the film/buried oxide interface for samples annealed at 1285°C.

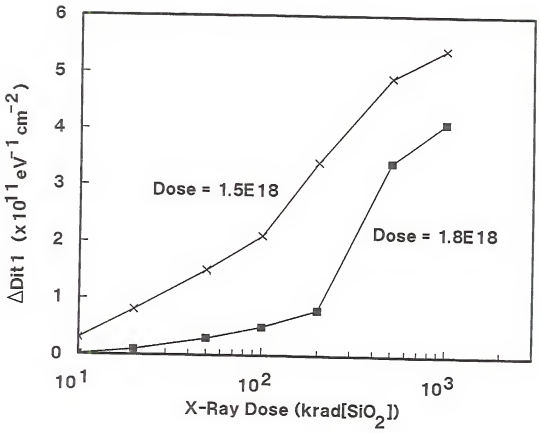


Figure 4.17. Generation of interface traps at the film/buried oxide interface for samples annealed at 1285°C for 6 hours.

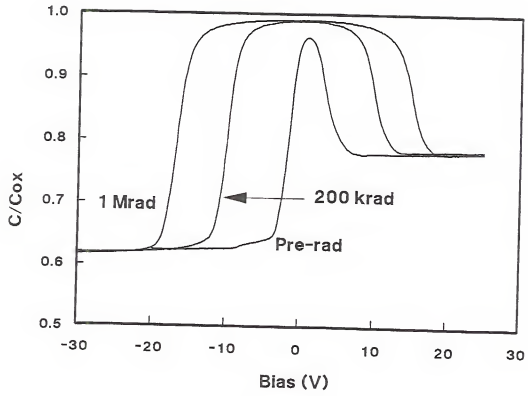


Figure 4.18. Typical pre- and post-irradiation C-V curves for SIMOX samples with an oxygen dose of 1.8×10^{18} cm^{-2}.

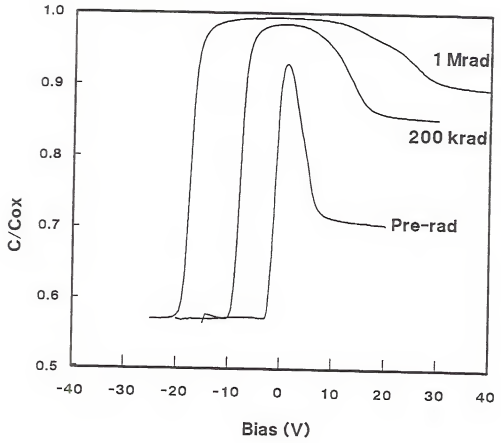


Figure 4.19. Typical pre- and post-irradiation C-V curves for SIMOX samples with three implants of 0.5×10^{18} cm^{-2}.

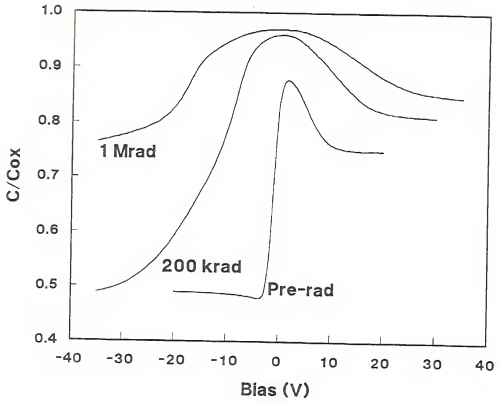


Figure 4.20. Typical pre- and post-irradiation C-V curves for a single implant of 1.5×10^{18} cm^{-2}.

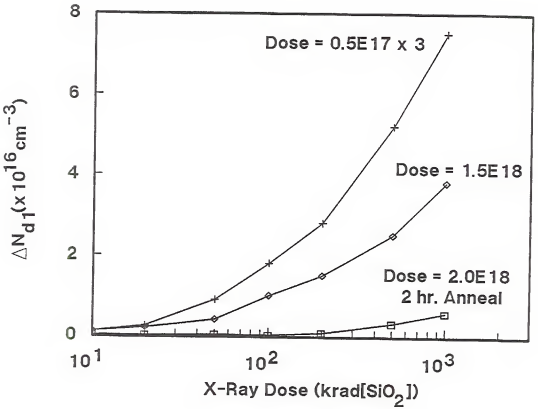


Figure 4.21. The donor enhancement effect, as a function of X-ray dose.

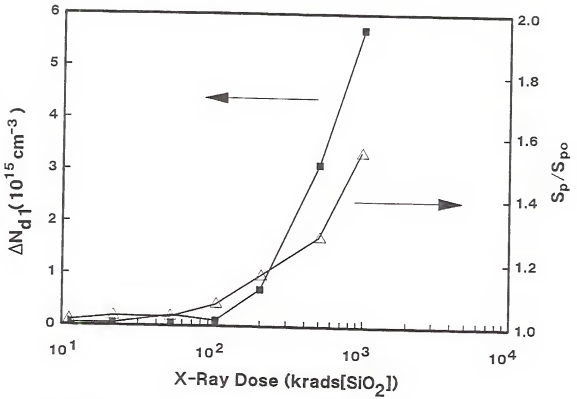


Figure 4.22. The correlation between the donor enhancement effect and the degradation in the subthreshold slope. The sample had an implant dose of 2.0×10^{18} cm^{-2}, and was annealed at 1250°C for 2 hours.

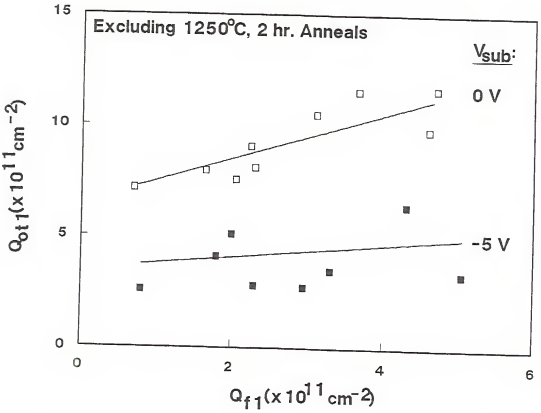


Figure 4.23. The correlation between the densities of the post-irradiation trapped charge and pre-irradiation fixed oxide charge, for the film/buried oxide interface.

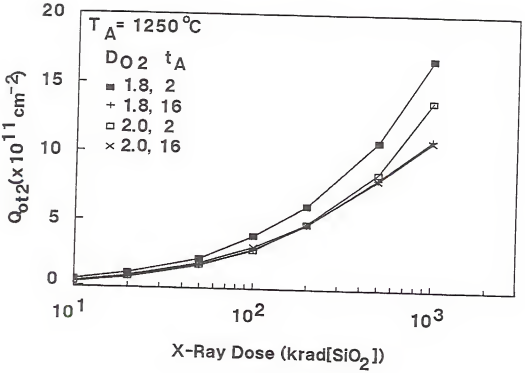


Figure 4.24. Post-irradiation charge trapping at the substrate/buried oxide interface for samples annealed at 1250°C.

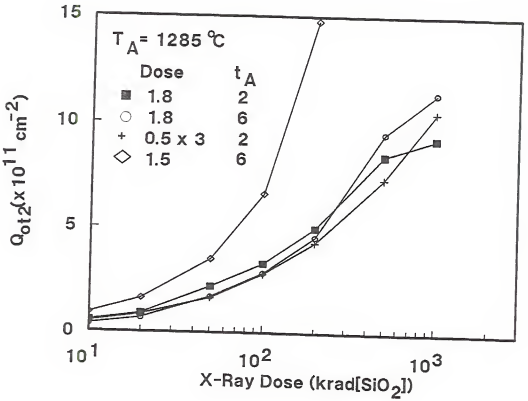


Figure 4.25. Post-irradiation charge trapping at the substrate/buried oxide interface for samples annealed at 1285°C.

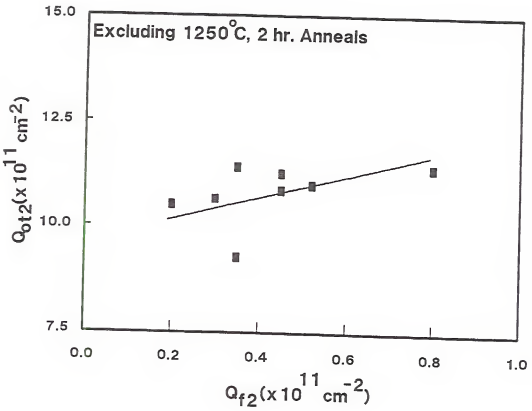


Figure 4.26. The correlation between the densities of the post-irradiation trapped charge and pre-irradiation fixed oxide charge, for the substrate/buried oxide interface.

CHAPTER 5

HIGH ELECTRIC FIELD STRESSING OF THE BURIED OXIDE LAYER

In Chapter 4, ionizing radiation was used to inject carriers into the buried oxide. In the present chapter, the effects of high electric fields are investigated. In particular, samples annealed at 1285°C are studied. This investigation is relevant to the reliability of the buried oxide in high voltage devices as well as in electrostatic discharge events. In addition, further understanding of the buried oxide defects is gained.

5.1 Fowler-Nordheim Tunneling

There are two methods of electrically introducing carriers into the oxide. The first is by hot carrier injection. In this approach, a large electric field is created at the silicon surface, so that electrons or holes are accelerated at the surface to attain sufficient energy the surmount the energy barrier at the Si/SiO_2 interface. This can be accomplished with a reverse biased p-n junction or by pulsing the interface into deep depletion. The second method is Fowler-Nordheim (F-N) tunneling. In F-N tunneling, the electric field across the oxide is high enough that the carriers can tunnel from the Si conduction band into the oxide conduction band. This is illustrated in Fig. 5.1. The barrier height for F-N injection is 3.3 eV for electrons, but 4.5 eV for holes, so that only electrons can be injected by this means. In this study, F-N tunneling is employed. Next, the expression for F-N tunneling is derived.

The tunneling current is equal to the product of the number of carriers available for tunneling and the transmission probability per electron, and can be written as [78]

$$J = qfNQ \tag{33}$$

where J is the current density, q is unit charge, f is the fraction of carriers in the lowest subband (equal to 0.626 at 300 K for < 100 > silicon), N is the number of electrons in the accumulation layer, and Q is the transmission probability per unit electron. The number of electrons in the accumulation layer can be obtained from electrostatic evaluation of the capacitor, and is equal to (assuming negligable charge in the oxide)

$$N = \frac{\epsilon_{ox} E_{ox}}{q} \tag{34}$$

where ϵ_{ox} is the dielectric constant of the oxide and E_{ox} is the electric field across the oxide. The transmission probability is given by

$$Q = \frac{q^2}{8\pi h \epsilon_{ox} \phi_B} \frac{m}{m_{ox}} E_{ox} T \tag{35}$$

In the above equation, h is Planck's constant, ϕ_B is the barrier height, m_{ox}/m is the effective electron mass in the SiO_2 bandgap, equal to 0.5, and T is the transmission coefficient. The expression for T can be found using the WKB approximation, and is [79]

$$T = \exp\left(\frac{-8\pi(2m_{ox}q)^{1/2}}{3hE_{ox}}(\phi_B)^{3/2}\right) \tag{36}$$

In the above equation, it is assumed that the electrons are all in the bottom of the conduction band. Combining the above equations, one can write an emipirical expression for the tunneling current

$$J = E_{ox}^2 C_1 \exp\left(-\frac{C_2}{E_{ox}}\right) \tag{37}$$

where

$$C_1 = \frac{m/m_{ox}q^2N}{8\pi h\epsilon_{ox}\phi_B} \tag{38}$$

and

$$C_2 = \frac{8\pi(2m_{ox}q)^{1/2}}{3h}(\phi_B)^{3/2} \tag{39}$$

For tunneling into an ideal thermal oxide, C_2 is equal to 283 MV/cm. The magnitude of the electric field required for F-N tunneling is very sensitive to the quality of the emitter/oxide interface. For high quality oxides, the minimum field is well over 7 MV/cm. For oxides grown on rough Si surfaces, such as polysilicon, F-N tunneling has been seen for fields as low as 2 MV/cm. Electron injection by F-N tunneling can alter the oxide charge in two ways. The first is the trapping of electrons by initially neutral traps. The second way is by bond breaking, as the electrons are very energetic. Interface traps and positive charge can be generated in this way. Using structures in which the oxide electric field and electron current could be varied separately, DiMaria [80] and Hsu et al [81] both found that the minimum electric field required for the generation oxide damage (for thermal oxides) is 1.5 MV/cm.

5.2 Experimental Details

Buried oxide capacitors were formed using the quick-turnaround technique (see Section 3.3). The samples investigated included the previously-discussed samples annealed at 1285°C for 6 hours. Two approaches to stressing were taken. The first was ramp I-V measurements, where the voltage was ramped at a rate of 0.5 V/s. The second approach was to apply a constant dc bias for 1 hour. The bias stresses were done at voltages ranging from 50 to 150 V. In both cases C-V measurements were taken immediately before and after stressing.

5.3 Results

5.3.1 Sample S5109

We begin a look at the results by examining the effects of high-field stress on sample S5109. This sample had an implant dose of 1.8×10^{18} cm^{-2}, and was annealed at 1285°C for 6 hours. In Fig. 5.2, typical ramp I-V measurements are shown for S5109. Several aspects of the curves should be pointed out. First, for lower biases, a shallow-slope region is seen. This corresponds to an ohmic region. Typical resistivities are 10^{12} – 10^{13} Ω-cm. At higher biases, the current is seen to jump up. As will be discussed below, this corresponds to the onset of F-N tunneling. Next, a big drop in the current is seen when the voltage is ramped down. This is due to the trapping of electrons in the bulk of the oxide. The trapped electrons generated an internal electric field that opposes the applied field, increasing the voltage necessary to maintain a given injection current. Finally, it is seen that the injected current density is much higher for positive biases (which corresponds to injection from the S/O interface) than for negative biases (injection from the F/O interface). We now discuss these phenomena more fully.

A closer examination of the I-V curves in the low field (< 2 MV/cm) region shows that curves exhibit ohmic behavior. The oxide resistivity can be calculated from the slope of the I-V curve, and the result is that for the better oxides, ρ is around 10^{12} – 10^{13} Ω-cm. This is slightly lower than the value of 10^{14} – 10^{16} Ω-cm expected for thermal oxides. It is also seen in Fig. 5.2 that the oxide resistivity tends to increase slightly after being stressed. This is due to the presence of trapped electrons in the oxide, which oppose the applied field.

In Fig. 5.2, it is seen that after a certain voltage threshold, the current sharply increases. The cause of this increase is the onset of F-N tunneling. To show that the electron injection mechanism is F-N tunneling, we plot $\ln(J/E^2)$ versus $1/E$ in Fig. 5.3. At higher biases, a straight line is seen, showing that F-N tunneling is indeed

the mechanism. From Fig. 5.3, one can estimate the threshold field for the onset of F-N tunneling. The resulting threshold fields (E_{FN}^{+} and E_{FN}^{-}) are 2.6 MV/cm for injection from the substrate and 2.9 MV/cm for the film. An additional difference is that a much steeper slope is seen for injection from the S/O interface. These values are much lower than those obtained with good quality thermal oxides. This is the opposite of what one would expect, since from Eq. (37), the slope is proportional to the effective barrier height. A greater slope would be expected for interfaces with higher E_{FN}. For example, good quality thermal oxides require fields of well over 7 MV/cm for F-N tunneling, and have a slope of 283 MV/cm. In Fig. 5.3, the slopes are 36 and 19.5 MV/cm for positive and negative bias injection, respectively.

The next aspect of the ramp I-V curves to be discussed is the sharp drop of the current during the ramp down portion of the curve. This effect is well known, and is due to the trapping of electrons in the oxide. The energy barrier between the Si and SiO_2 conduction bands is insensitive to trapping at the Si/SiO_2 interface, but sensitive to trapping in the bulk. The presence of electrons trapped in the bulk of the oxide creates an internal field opposing the applied field. Thus a higher applied field is required to maintain a given current. Thus, using Fig. 5.2, one can calculate the density of trapped electrons for both ramp stresses. The result is 1.7×10^{12} e-/cm^2 for injection from the F/O interface and 1.6×10^{12} e-/cm^{-2} for injection from the S/O interface. Note that while the injected current is sensitive primarily to bulk electronic charge, C-V measurements are sensitive to the net oxide charge. Thus, to analyze the total degradation of the buried oxide, C-V curves were taken before and after the ramp I-V stresses. The results can be seen in Fig. 5.4. In the inset, the corresponding values for net oxide charge and interface trap densities are shown, as well as the bulk electron trapping. Several trends can be seen. The first is that the degradation at an interface increases when the injection is from that interface. However, irrespective of the polarity of the injecting bias, there is always significantly

greater degradation at the S/O interface than at the F/O interface. Since both Q_{ot2} and ΔD_{it2} are very high, the bonding at the S/O interface must be weaker than at the F/O interface. Another interesting aspect of the C-V curves is that despite the high density of trapped electrons, the net oxide charge is still positive.

To examine the effects of high-field stress more closely, constant voltage stresses were applied to the BOXCAPs for 1 hour. Several different voltages were studied, for both positive and negative polarities. The results are summarized in Fig. 5.5. In this figure, it is again seen that more damage is created at the S/O interface than at the F/O interface for both bias polarities. For injection from the F/O interface, the threshold voltage for generating damage at the F/O interface (E_{df}) is 2.8 MV/cm, while the threshold for generating damage at the S/O interface (E_{ds}) is 2.0 MV/cm. Similarly, for positive stressing biases, the thresholds for generating damage at the F/O and S/O interfaces are $E_{df} = 2.8$ MV/cm and $E_{ds} = 2.0$ MV/cm. This difference is significant, and strongly indicates that the bonding is different at the two buried oxide interfaces. The bonding difference may be due in part to the large density of Si precipitates in the buried oxide layer near the S/O interface. It is particularly interesting that E_{ds} is below the threshold voltage for F-N tunneling from the film. This indicates that a high percentage of the tunneling electrons are generating the defects, implying a large cross section for defect generation. For both stressing polarities, a rough correlation is seen between Q_{ot} and ΔD_{it} for a given interface, although Q_{ot} increases more rapidly than does ΔD_{it}. For positive biases, the correlation between Q_{ot} and ΔD_{it} is seen at lower fields. At higher fields, however, ΔD_{it2} actually begins to decrease. The maximum occurs around 2.5 MV/cm. For the F/O interface, at higher fields, the net charge trapping becomes negative.

An interesting question is the correlation of the bias stress and irradiation stress results. For this sample, significant densities of interface traps were generated under both types of stress. However, a major difference is seen in the charge trapping

behavior. For irradiation under a 0 V bias, the trapping of positive charge was nearly identical for both interfaces, with only a 10% difference. For bias stress, the S/O interface has much higher positive charge densities than does the F/O interface. The difference in the positive charge generation shows that the physical origin of the defects are different.

5.3.2 Sample MI10

A similar analysis was performed on sample MI10. In Fig. 5.6, the ramped J-V curves are shown. The curves are very symmetrical with respect to the stressing polarity. This is surprising, since a row of oxide precipitates is seen adjacent to the F/O interface, while the S/O interface is relatively smooth. In addition, the slope of the curve after the onset of F-N tunneling is so shallow, that it is difficult to separate it out from the ohmic portion of the curve. However, a drop in the current is seen on the ramp down, indicating electron trapping. Furthermore, as seen in Fig. 5.7, a linear J/E^2 versus $1/E$ plot is obtained on the semi-log graph. From Fig. 5.7, it can be seen that $E_{FN}^{+} = 2.6$ MV/cm while $E_{FN}^{-} = 2.8$ MV/cm. As might be expected from the lower threshold voltage, a greater number of electrons are trapped for injection from the substrate. As seen in the C-V curves in Fig. 5.8, this results in enhanced degradation for positive bias injection. Surprisingly, more defects are generated at the F/O interface for injection from the substrate than for injection from the film. This is true for the S/O interface also. A comparison of MI10 and S5109 shows that although Q_{it1} and $\triangle D_{it1}$ are of similar values for injection from the substrate, S5109 otherwise has greatly enhanced degradation, especially for the S/O interface. This is partly due to the previously discussed low damage threshold for the S/O interface for S5109. However, even for injection from the film, for which the electron fluence and peak electric fields are similar for the two samples, S5109 has an order of magnitude greater degradation. This shows that the multiple implant process greatly enhances the hardness of the buried oxide.

Hour-long constant bias stresses were also performed on MI10, the multiple implant sample. The resulting analysis of oxide charge and interface traps can be seen in Fig. 5.9. The degradation is seen to be very symmetrical with respect to the stressing polarity. The threshold for generating damage appears to be equal for both buried oxide interfaces, and equal to around 2.8 MV/cm. However, after the onset defect generation, the degradation of the S/O interface increases very fast with electric field, for both bias polarities. For positive stresses, there appears to be an annealing out of defects at the S/O interface for fields greater than 3.7 MV/cm. A major difference between the ramp stress and the constant bias stress is the behavior of the interface traps. For ramp stresses, roughly equal trap densities were generated at each interface. With constant bias stress, however, $\Delta D_{it2} >> \Delta D_{it1}$. It is also seen that the generation of interface traps and net oxide charge tend to track each other well. Again, comparing Fig. 5.9 to Fig. 5.5 shows that S5109 is much more degraded by high electric field stress than MI10. In Section 4.4 it was seen that at 1 Mrad, MI10 had much less positive charge trapping than S5109. Thus the degradation trends (as a function of processing) are similar for both types of stress.

5.3.3 Sample S4419

Next, the analysis of the low-dose, single-implant sample, S4419, is discussed. In Fig. 5.10, a typical J-E curve is shown for this wafer. Contrary to results for the other samples, enhanced injection is seen for negative biases, corresponding to injection from the film. Not only is the current significantly higher than for the other SIMOX samples, but the F-N tunneling threshold voltage is clearly lower. This is expected, as TEMs show this sample to have a very rough F/O interface. The large voltage shift for negative biases also indicates a large number of trapped electrons. In Fig. 5.11, the F-N graph is shown, again showing that the injection mechanism is F-N tunneling. From this graph, E_{FN}^{+} and E_{FN}^{-} are determined to be 2.6 and 1.8 MV/cm, respectively. The corresponding pre- and post-stress C-V curves are shown in Fig.

5.12. A severe distortion of the C-V curves is seen. This is due to a net negative charge, as compared to the net positive charge trapping seen for S5109 and MI10. The distortion of the post-stress curves makes the curve fitting approach difficult, especially for the F/O interface parameters. Note that negative charge trapping is seen even for injection from the substrate, for which the injected fluence is of a value similar to the other samples. This indicates that the net negative charge is due to the reduced generation of positive charge, rather than to enhanced electron trapping.

With the difficulty in fitting the post-stress C-V curves at high biases, the constant bias study focused on lower electric fields. In this study, the injected electron dose was monitored, and the stressing periodically interrupted and C-V measurements performed. The resulting analysis is shown in Fig. 5.13. The main points of the graph are that the degradation at both interfaces is higher for injection from the film, and that the net charge trapping is negative, as seen for both oxide interfaces.

5.4 Discussion

The stressing studies are summarized in Table 5.1. The key results are discussed in the following section.

In the first column of Table 5.1, the values of E_{FN}^{+} are listed for the various oxides. Within experimental error, they are the same. For injection from the film, however, some difference is seen among the samples, with S4419 having a significantly lower E_{FN}^{-}. This follows the same trend seen in the overall SIMOX characterization program, in which the S/O interface has been found to be much less sensitive to changes in processing than the F/O interface. Surprisingly, despite the similarity of the threshold voltages for tunneling from the substrate, the values for C_2^{+} vary significantly. Noting that ideal oxides have a value of 283 MV/cm, one can see that S4419, which has the roughest looking interface, has the highest value for C_2^{+}. For C_2^{-}, S4419 again has the highest value, despite having a low F-N threshold field. The

explanation may be that the potential barrier at the Si/SiO_2 interface is different for SIMOX oxides than for thermal oxides.

A good question is how the degradation reslates to the microstructure of the buried oxide. To examine the question, TEMs were taken of all three samples. These pictures are shown in Figs. 5.14 – 5.16. S5109 is seen to have rough BOX interfaces, with small SiO_2 protrusions into the Si film. Si islands are seen in the BOX near both the F/O and S/O interfaces, but the ones near the S/O interface are bigger and more numberous. MI10, on the other hand, has very few precipitates in the BOX. However, the interfaces are quite rough, and oxide protrusions are seen in the Si film. Finally, S4419 has a very high density of Si islands in the BOX, near both interfaces. Again, the oxide interfaces are rough, especially the F/O interface. If the microstructure of these sampels is compared to the data in Table 5.1, it is seen that there is little correlation between the microstructure and the F-N threshold field. It is particularly clear that the Si islands have no effect. For example, for the S/O interface, the surface roughness is approximately equal for the samples. The major difference is the number of islands. However, it is seen that E_{FN}^{+} is the same for all of the samples. Likewise, the surface roughness appears to have little effect on the threshold field for the top BOX interface. For all three samples, the F/O interface appears to be much rougher than the S/O interface. Yet, E_{FN}^{-} is higher for the F/O interface except for S4419. Efforts are underway to measure the actual barrier heights, to see if the Si/SIMOX interface actually has a lower barrier than Si/thermal oxides. However, it has been shown that the barrier height for polyoxides and Si-rich CVD oxides is unchanged from thermal oxides.

During the course of the investigation, it was noticed that there was a wide spread of oxide leakages. To investigate this more closely, the leakage current at -15 V was measured for a large number of BOXCAPs, from both S5109 and S4419. The resulting distribution of leakage currents is graphed in Fig. 5.17. Surprisingly, three

distinct ranges are seen are seen: (R1) 0 to 100 pA; (R2) 1 to 10 μA; and (R3) > 10 μA. Clearly, there are three separate leakage mechanisms. R1 is due to the intrinsic dielectric quality of the oxide. It includes oxides with a resistivity greater than 10^{12} Ω-cm. R3 consists of buried oxides that behave essentially as a short circuit. The mechanism for R3 is most likely due to large pinholes created by the presence of large particulates on the surface during oxygen implantation [82]. The mechanism for R2 is not as clear. A likely cause is the presence of Si "pipes" in the buried oxide. Other groups have proposed the presence of these pipes after finding anomalous results when etching the buried oxide. The source of these pipes is somewhat controversial, and may be due to the presence of small particulates on the sample during implantation [83] or to anomalous high temperature annealing behavior [84].

5.5 Summary

I-V, C-V, and constant bias measurements have been used to stress SIMOX buried oxide layers and to determine the amount of post-stress degradation. For all of the samples studied, relatively low electric fields were sufficient inject electrons via Fowler-Nordheim tunneling. The threshold voltages for injection from the substrate were essentially identical for all of the samples. The low-dose, single implant sample was found to have enhanced injection from the film, while the standard dose sample was found to have reduced injection from the film.

The degradation characteristics of the three samples were found to be dramatically different. For example, the net oxide charge was negative for the low-dose single implant sample, but positive for the others. For both the multiple implant and standard dose samples, greater degradation was seen for the S/O interface than for the F/O interface; however, for both interfaces, the standard dose sample exhibited greater degradation.

Table 5.1 Summary of Ramp I-V Measurements. The quantity E_{FN} is the threshold field for F-N tunneling, C_2 is the slope exponential constant in the empirical F-N tunneling equation, and E_d is the threshold field for degradation at an interface. A $^+$ refers to injection from the substrate, while $^-$ refers to injection from the film. The subscript variables f and s refer to the F/O and S/O interfaces, respectively. Finally, N_{sis} and N_{fis} refer to the number of Si islands in the BOX near the S/O and F/O interfaces, respectively.

Sample	E_{FN}^{+}	E_{FN}^{-}	C_2^{+}	C_2^{+}	E_{df}	E_{ds}	N_{sis}	N_{fis}
	MV/cm	MV/cm	MV/cm	MV/cm	MV/cm	MV/cm		
S5109	2.6	2.9	36.0	19.5	2.8	2.0	20	14
MI10	2.6	2.8	9.2	10.4	2.8	2.8	1	0
S4419	2.6	1.8	49.2	28.3	1.8	1.8	50	40

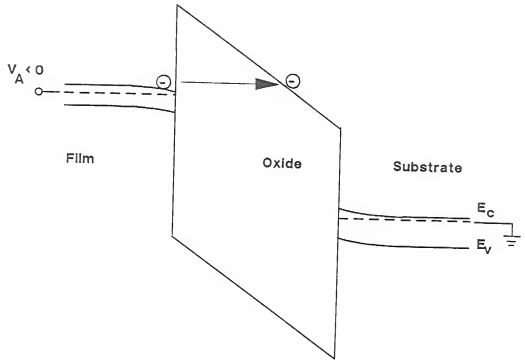


Figure 5.1. Energy band diagram for Fowler-Nordheim tunneling from the film.

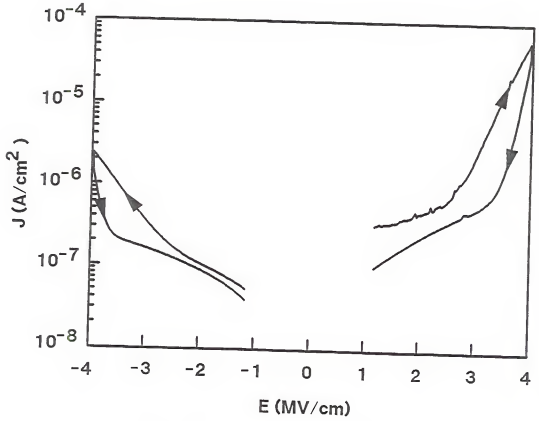


Figure 5.2. Typical J-E curves for sample S5109.

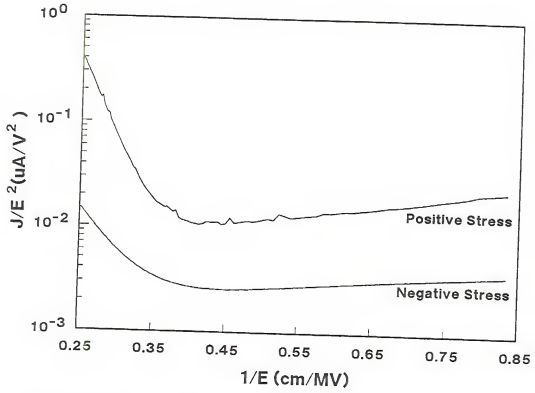


Figure 5.3. Fowler-Nordheim plot of the J-E curves in Fig. 5.2, with straight lines seen at the higher biases.

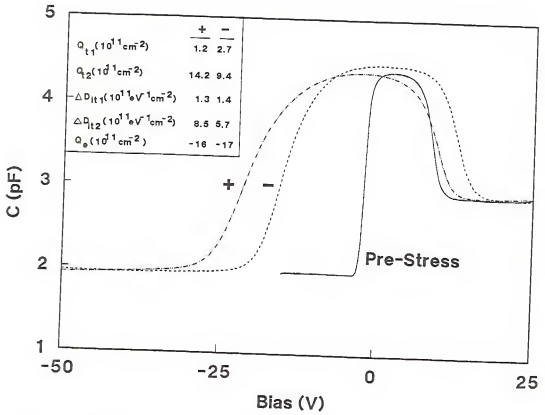


Figure 5.4. C-V curves before and after the ramp I-V stress shown in Fig. 5.2. Q_e refers to the density of electrons trapped in the bulk of the oxide, as calculated from the shifts in the I-V curves. The symbols "+" and "-" refer to positive and negative bias injection, respectively.

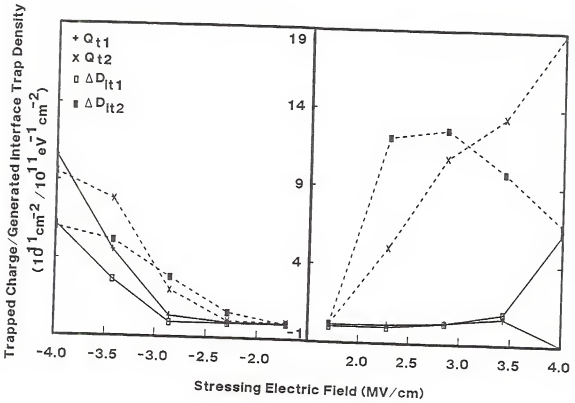


Figure 5.5 The results of 1 hour constant bias stress on sample S5109.

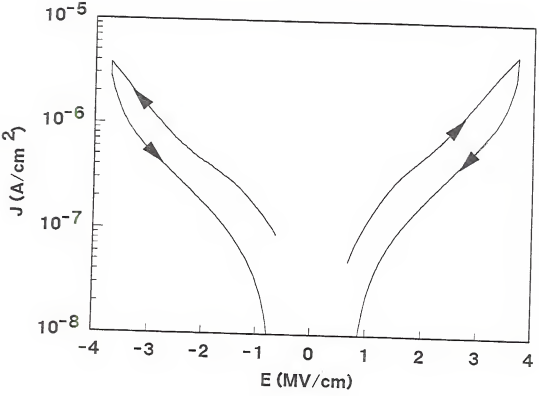


Figure 5.6. Typical J-E curves for sample MI10.

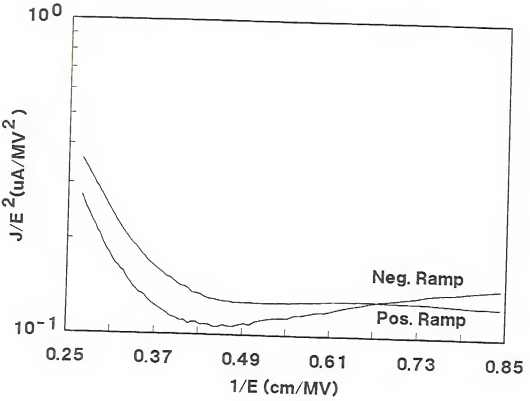


Figure 5.7. Fowler-Nordheim plot of the J-E curves in Fig. 5.6, with straight lines seen at the higher biases.

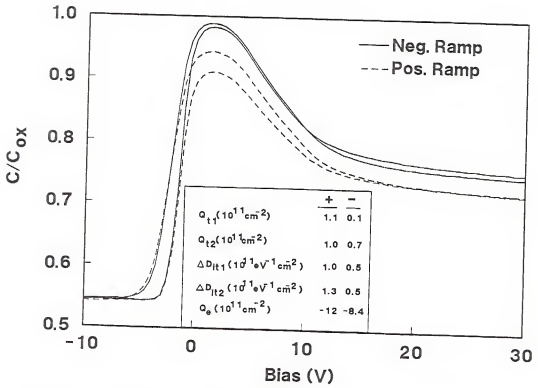


Figure 5.8. C-V curves before and after the ramp I-V stress shown in Fig. 5.6. Q_e refers to the density of electrons trapped in the bulk of the oxide, as calculated from the shifts in the I-V curves. The symbols "+" and "-" refer to positive and negative bias injection, respectively.

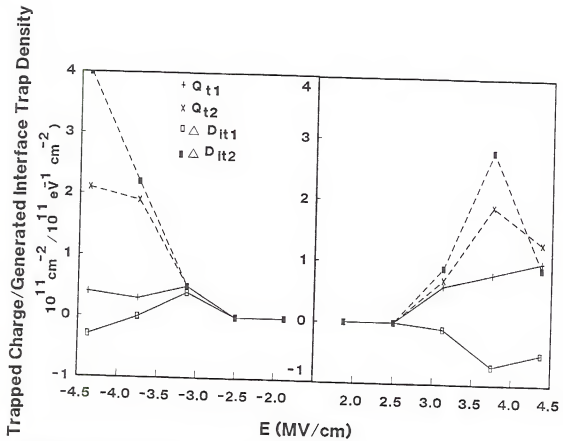


Figure 5.9 The results of 1 hour constant bias stress on sample MI10.

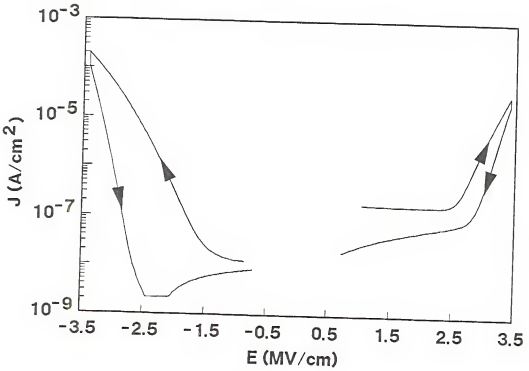


Figure 5.10. Typical J-E curves for sample S4419.

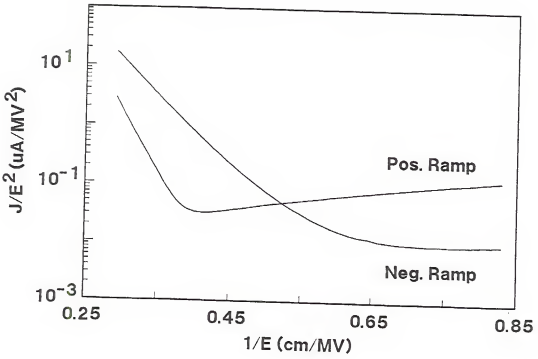


Figure 5.11. Fowler-Nordheim plot of the J-E curves in Fig. 5.10, with straight lines seen at the higher biases.

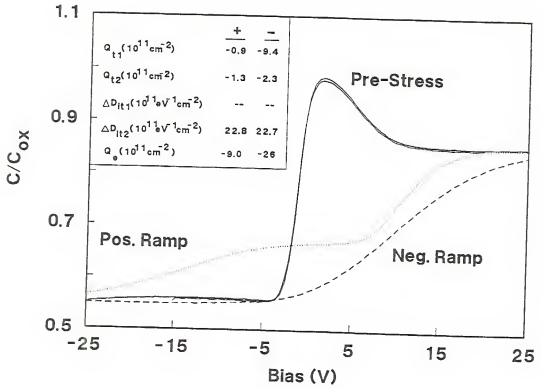


Figure 5.12. C-V curves before and after the ramp I-V stress shown in Fig. 5.10. Q_e refers to the density of electrons trapped in the bulk of the oxide, as calculated from the shifts in the I-V curves. The symbols "+" and "-" refer to positive and negative bias injection, respectively. Values could not be obtained for D_{it1}.

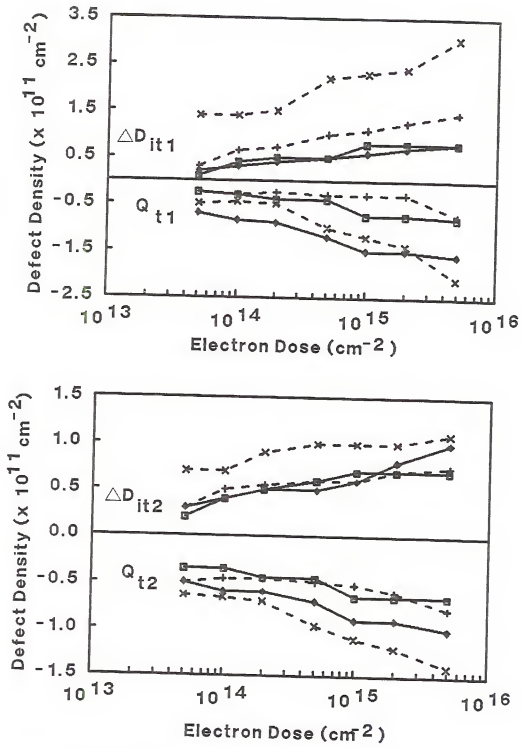


Figure 5.13. The result of constant bias stress on S4419. The current was monitored to obtain the electron dose.

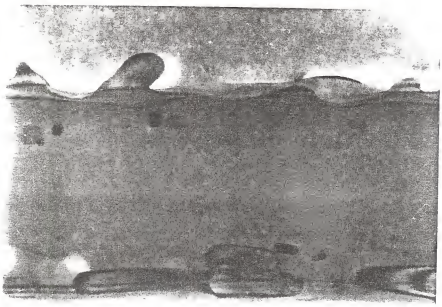


Figure 5.14. TEM of S5109. The magnification is 150,000.

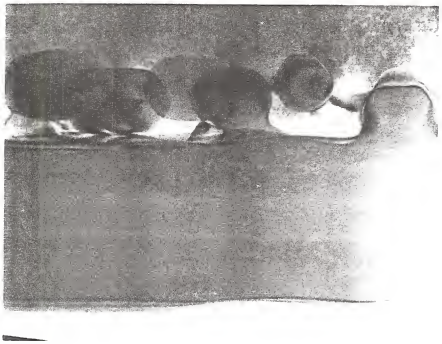


Figure 5.15. TEM of MI10. The magnification is 150.000.

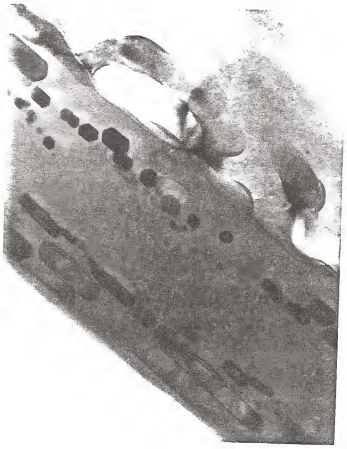


Figure 5.16. TEM of S4419. The magnification is 150.000.

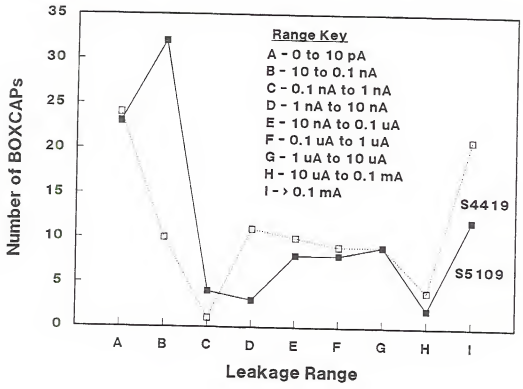


Figure 5.17. Distribution of buried oxide leakages.

CHAPTER 6
THE DUAL BEAM OPTICAL MODULATION TECHNIQUE

The success of Japanese semiconductor manufacturers has made it clear that reducing production costs and improving yields are key elements in the timely and cost-effective fabrication of integrated circuits. Indeed, stiff competition in the semiconductor industry and increased demands by its customers have made it more important than ever to deliver high quality parts at low prices. This, however, is quite difficult. The electrical characteristics of integrated circuits are very sensitive to drifts in the process parameters of the fabrication equipment. When processing equipment early in the fabrication sequence goes out of control, the results may not be detected for weeks or even months – after significant funds have been invested in the wafer. Thus, it is becoming clear that the performance of each piece of equipment must be monitored on a regular basis. Both batch-to-batch and across-the-wafer uniformity need to be monitored. Instruments are commercially available that can determine the thicknesses of multilayered films or detect the presence of particles on the surface. However, even if the films are deposited uniformly, contamination may be present. This contamination can only be detected by electrical measurements. However, there are very few commercially available systems capable of nondestructively monitoring the electrical quality of semiconductor wafers.

The area of SIMOX circuit fabrication is a particularly important application for nondestructive evaluation. The technological problems involved in fabricating high quality SIMOX wafers consistently on a production basis are great. Since the SIMOX process is a young technology, there are still problems to be worked out. As a result, there is a significant need for nondestructive techniques for the evaluation of incoming

SIMOX lots.

In this chapter, a prototype instrument is developed for the nondestructive measurement of the minority carrier lifetime in semiconductor materials and devices, based on the dual-beam optical modulation (DBOM) technique. This method is based on the change in the transmission of infrared light through a wafer due to absorption by free carriers. The excess carriers are generated by one light source (the pump beam) while the change in the transmission of the second source (the infrared probe) is monitored.

6.1 Nondestructive Evaluation Techniques

In the competitive environment of semiconductor manufacturing, it has become very important to maximize the efficiency of each step in the fabrication process. Recognition of this fact has spurred the development and adoption of computer aided manufacturing (CAM), just-in-time (JIT) manufacturing, and statistical process control (SPC). Even today, process control consists largely of testing the finished chip. Wafers are pushed through the fabrication line until the yield becomes unacceptable. Determining the problem is a lengthy process consisting of testing each piece of equipment. Meanwhile, the fab line is shut down, and the wafer lots between the out of control equipment and the one at probe must be scrapped or at least reworked. Clearly, this is a waste of money. Thus, the performance of each piece of equipment must be checked on a regular basis. This is especially true of equipment used early in the fabrication sequence.

For routine monitoring of processes early in the fabrication sequence, it is imperative that the analysis techniques must be quick, reliable, and nondestructive. There are two approaches to characterizing the performance of process equipment. The first is to measure the critical dimensions of the film formed by the process. For example, ellipsometry measurements are used to insure that thickness of gate oxides falls within

the specified limits. While many of these techniques are optical, and thus nondestructive, they do not give any information on the electrical quality of the samples under study. Even if the thickness of the gate oxide is acceptable, contamination may have been introduced during the oxide growth. This contamination will degrade the silicon, but it will not be detectable by ellipsometry. This brings us to the second approach, electrical measurements. There are a large number of electrical measurements that can be used to characterize the output of the process. They include measurements of capacitor relaxation times, the voltage decay of reverse bias p-n junctions, and photocurrents. However, these techniques all require an electrical contact to the sample under study, and so are destructive. Thus, an all-optical approach is required.

The only standard measurement system for nondestructive electrical measurements is the SPV (surface photovoltage) technique [85]. The SPV method consists of shining variable wavelength light on the sample, and measuring the resultant photovoltage via a capacitive contact. As the wavelength is varied (usually between 800 and 1000 nm), intensity of the light is varied to keep a constant photovoltage. Alternately, the ratio the light intensity to the photovoltage is recorded. Either way, the variable of interest is plotted versus the inverse of the absorption coefficient, and the diffusion length obtained from the x-axis intercept. However, there are some problems with the SPV technique. The first is that there is great variability between the different instruments. This makes it difficult to calibrate an individual instrument, and makes it use unreliable. The second problem is that light in the wavelength range 800 to 1000 nm is deeply penetrating, and so it cannot be used to study the ultra thin films encountered in SOI materials. Back surface SPV measurements have been proposed monitoring the contamination of SIMOX wafers, but the technique can only be applied to as-implanted wafers. A technique utilizing short wavelength light sources is needed.

6.2 Theory for the DBOM Technique

It is well known that infrared (IR) light is absorbed by free carriers. Indeed, several journal papers have been published in which the carrier lifetime is measured using the pump/probe approach [86,87,88]. The variations include steady-state or transient measurements, and intersecting the two beams in a perpendicular or parallel fashion. In our approach, steady state measurements are used. DBOM theory is applied to three separate cases. The first is the general case of bulk silicon. Next, theory for the analysis of SOI substrates from the front side is derived. Finally, the case of ultra thin films is considered.

6.2.1 Bulk silicon.

We begin by discussing the case of bulk silicon. The expression for the attenuation of light passing through an absorbing material is

$$I = I_o(1 - R)e^{-\alpha d} \tag{40}$$

where I_o is the incident intensity, R is the reflectivity, α is the absorption coefficient, and d is the thickness of the absorbing material. For silicon, the absorption of light with energy less than the bandgap (1.1 eV) is due to free carrier absorption. The absorption coefficient for free carriers is given by [89]

$$\alpha = \frac{\lambda^2 g q^3}{4\pi\epsilon c^3}\left[\frac{n}{m_n^2\mu_n} + \frac{p}{m_p^2\mu_p}\right] \tag{41}$$

where λ is the wavelength of the light, g is a material constant, approximately equal to 1, q is the unit electron charge, ϵ is the dielectric constant of silicon, c is the speed of light, n and p are the concentrations of electrons and holes, $m_{n,p}$ is the conductivity effective masses for electrons and holes, and $\mu_{n,p}$ is the mobility of electrons and holes. It is seen in Eq.(4) that α is linearly proportional to the concentration of electrons and holes. If the carriers are injected into the sample (e.g. the pump beam), the

change in the absorption coefficient will be

$$\Delta\alpha = [\sigma_n + \sigma_p]\Delta n \tag{42}$$

where

$$\sigma_{n,p} = \frac{2\lambda g q^3}{4\pi\epsilon c^3 m_{n,p}^2 \mu_{n,p}} \tag{43}$$

is the free carrier absorption cross section. To further simplify the analysis, the cross section is written as $\sigma = \sigma_n + \sigma_p$. The transmission of light through the wafer can now be written as

$$I = I_o e^{-\alpha d} e^{-\sigma \Delta n x} \tag{44}$$

where x is the thickness of the absorbing medium. Defining $I_{dc} = I_o e^{-\alpha d}$ as the transmitted power without attenuation by excess free carriers, the change in the transmitted power is

$$\Delta I = I_{dc}(1 - e^{-\sigma \Delta n x}) \tag{45}$$

Following the exponential decay of the pump beam, the steady state concentration of carriers decays exponentially into the sample:

$$\Delta n = (1 - R)\gamma\phi\tau_n / L_n \ \exp(-z/L_n) \tag{46}$$

In the above equation, R is the reflectivity, γ is the quantum efficiency, ϕ is the photon flux density of the pump beam, τ is the carrier lifetime, L is the carrier diffusion length, and z is the distance into the sample. Integrating the excess carrier density over the thickness of the wafer then gives

$$\frac{\Delta I}{I_{dc}} = -(1 - R)\gamma\sigma\phi\tau' \tag{47}$$

where τ' is the effective lifetime, including surface recombination effects. ΔI, I, R, and ϕ are measurable quantities. The cross section is easily obtained from published tables, and γ is typically assumed to be 1.

Some problems arise when applying the technique to SOI wafers. First, the thickness of the Si film relative to the pump beam absorption depth must be considered. If the film thickness (t_{si}) is much greater than α, then the contribution from the substrate can be neglected. If $t_{si} < \alpha$, then the contribution of the film can be neglected. In the latter case, the substrate lifetime is obtained, and the DBOM technique can be used as a process contamination monitor. In the event that t_{si} is greater than α, the relative values of t_{si} and the diffusion length, L, are still important. If t_{si} is less than L, then the number of carriers available to absorb the probe beam will be reduced, and the sensitivity of the experiment reduced.

6.2.2 SOI Substrate measurement from the Front Side.

We now discuss the simple case when the contribution of the film to the DBOM signal can be ignored. For this situation, one needs to take into account aborption of the pump beam by the film and reflection of the pump beam at the buried oxide interfaces in order to correctly calculate the power of the pump beam reaching the interface. In addition, we consider the general case for which the pump beam is not incident perpindicular to the wafer surface. However, multiple reflections are neglected, and the pump beam is assumed to travel parallel to the plane perpindicular to the wafer surface.

Consider the SOI structure shown in Fig. 6.1. A beam of power I_o is incident on the wafer at an angle of θ_1. The transmission of light through an interface can be written as

$$t = \frac{k_{tx}}{k_{ix}}|T^2| \tag{48}$$

where $k_{t,ix}$ are the transmission and reflection vectors of the light, with

$$k = xk_x + yk_y + zk_z \tag{49}$$

and the magnitude of k is equal to $\omega^2\mu\epsilon$. The quantities ω, μ, and ϵ are the frequency, permeability, and dielectric constant, respectively. The transmission coefficient, T, is equal to

$$T = (\frac{2}{1 + \frac{k_{tx}}{k_{ix}}})^2 \tag{50}$$

Thus, I_1 can be written as

$$I_1 = I_o(\frac{k_{tx}}{k_{ix}})_1[\frac{2}{1 + (\frac{k_{tx}}{k_{ix}})_1}]^2 \tag{51}$$

where

$$(\frac{k_{tx}}{k_{ix}})_1 = \frac{(\frac{\epsilon_2}{\epsilon_1} - \sin^2\theta_1)^{1/2}}{\cos\theta_1} \tag{52}$$

As it travels through the Si film, the pump beam will be partially absorbed. Thus, the intensity of light reaching the film/BOX interface can be written as

$$I_1^* = I_1\exp(-\alpha l) \tag{53}$$

where α is the absorption coefficient and l is the path length through the Si film. Using Snell's law and from geometrical considerations, the path length is equal to

$$l = \frac{t_{si}}{\cos(\sin^{-1}((\frac{\epsilon_1}{\epsilon_2})^{1/2}\sin\theta_1))} \tag{54}$$

In a similar fashion, transmission at the film/BOX and BOX/substrate interfaces can be calculated. The results are

$$I_2 = I_1^*(\frac{k_{tx}}{k_{ix}})_2[\frac{2}{1+(\frac{k_{tx}}{k_{ix}})_2}]^2 \tag{55}$$

where

$$(\frac{k_{tx}}{k_{ix}})_2 = \frac{(\frac{\epsilon_3}{\epsilon_2} - \sin^2\theta_2)^{1/2}}{\cos\theta_2} \tag{56}$$

and

$$\theta_2 = \sin^{-1}[(\frac{\epsilon_1}{\epsilon_2})^{1/2}\theta_1] \tag{57}$$

Finally, I_3 can be determined:

$$I_3 = I_2(\frac{k_{tx}}{k_{ix}})_3[\frac{2}{1+(\frac{k_{tx}}{k_{ix}})_3}]^2 \tag{58}$$

where

$$(\frac{k_{tx}}{k_{ix}})_3 = \frac{(\frac{\epsilon_4}{\epsilon_3} - \sin^2\theta_4)^{1/2}}{\cos\theta_4} \tag{59}$$

and

$$\theta_4 = \sin^{-1}[(\frac{\epsilon_2}{\epsilon_3})^{1/2}\theta_2] \tag{60}$$

The above equations were used to generate a plot of I_3/I_o as a functions of the incident angle and the film thickness. The result is shown in Fig. 6.2. Clearly, one should minimize θ_1 and t_{si}. The large increase of I_3/I_o for $t_{si} = 0$ is due to the high reflection coefficient for the air/Si interface. Experimental results obtained for this type of measurement are discussed in Section 6.4

6.2.3 Ultra thin film analysis.

Clearly, since the number of excess carriers are reduced in ultra thin films (relative to bulk Si), a compensating factor needs to be determined. First, we determine the minimum Si film thickness required to generate a detectable DBOM signal for a given lifetime. Using Eqs. (8) and (9), and some algebra, the following equation is arrived at:

$$\tau[\exp(-t_{si}/L) - 1] > \frac{\Delta I/I}{(1-R)\gamma\sigma\phi} \tag{61}$$

If the pump beam is a 10 mW ultraviolet laser ($\lambda = 0.325$ μm), the pertinent values are R = 0.3, $\gamma = 1$, $\sigma = 1 \times 10^{-16}$ cm^{-2}, and $\phi = 5.2 \times 10^{17}$ cm^{-2}. The quantity $\Delta I/I$ is limited by the dymamic range of the lock-in amplifier, and is realistically equal to 10^{-7}. Using these values, the previous equation becomes

$$\tau[\exp(-t_{si}/L) - 1] > 2.75 \times 10^{-9} \tag{62}$$

Using a value of 10 cm^2/s for the diffusivity, the above equation can be used to find the minimum t_{si}. For $\tau = 1$ μs, $t_{si_{min}}$ is 0.085 μm, while for $\tau = 0.1$ μs, a value of 0.275 μm is obtained. Note that for bulk Si, the above equation indicates a minimum measureable τ of 3 ns. This derivation indicates that it should be fairly easy to obtain a DBOM signal on good quality ultra thin SOI films. However, second order effects need to be taken into account. The first is the high level injection of carriers by the pump beam. A typical UV source is a 10 mW HeCd laser. At this wavelength, the absorption coefficient for silicon is about 1.5×10^6. Thus, 90% of carriers are generated within 15 nm. The corresponding volume generation rate is 2×10^{23} electron-hole pairs/(cm^{3}s). This is a very high number. Many of the generated pairs will immediately recombine. Auger band-to-band recombination will also be important. Other carriers will be lost to surface recombination at the top surface. Thus, the effect will be to reduce the number of carriers that survive to

diffuse away from the surface into the body of the film. Finally, recombination at the film/BOX interface will further reduce the number of carriers. Thus, it appears that applying the DBOM technique to ultrathin SOI films will be difficult. Experimental results based on using a HeCd laser will be discussed below.

6.3 Experimental Details

A sketch of the DBOM set up is shown in Fig. 6.3. Clearly, the set up is very simple and inexpensive. It can easily be operated by a technician. The major problem is the aligment of the pump and probe beams on the surface of the wafer. However, careful alignment alleviates this problem. When measuring a wafer, I_{dc} is measured first by turning on the chopper by the microscope light, and measuring the resulting signal on the lock in. This chopper is turned off, and the chopper for the laser turned on. The resulting signal is ΔI. To minimize the effects of stray light from the laser, optical baffles were set up around the wafer.

6.4 Results

Essentially three types of measurements were made. The first was on relatively thick Si film wafers, the second was measurements on ultra thin Si film material with the HeNe laser (for substrate analysis), and the third was measurements on ultra thin Si film material with a UV laser (for film analysis).

6.4.1 Thick film SOI wafers.

Using a He-Ne laser operating at 632 nm measurements were performed on bulk and SIMOX wafers. Epilayers of 1.5 μm were grown on the SIMOX wafers. In addition an n^+ layer of 0.2 μm was diffused into the top surface (to facilitate ohmic contacts for other measurements). For Si films of this thickness, half of the incident pump power is absorbed in the film and half in the substrate. The results are shown in Table 6.1. The lifetime is low for the bulk wafer because it is a low quality dummy wafer. Surface

recombination effects also decrease the effective lifetime. For the SIMOX wafers, the lifetime shown is an average lifetime for the film plus substrate. Transmission electron microscopy (TEM) pictures were also taken of the samples. A good correlation was found between the lifetimes and the presence of oxide precipitates in the Si film, indicating some sensitivity to defects in the film. Because of the surface n^+ layer the UV laser could not be used on these SIMOX wafers. Since UV light is absorbed within 15 nm of the surface, all of the carriers are generated in the low lifetime region. To show that the measured signal was due to the modulation the IR beam by the free carriers, $\Delta I/I$ is graphed in Fig. 6.4. From Eq.(10), a straight line is expected. As seen in the Figure, a straight line is obtained.

6.4.2 Substrate lifetime measurements on ultra thin film samples.

In Section 6.4.1, the substrate and film lifetimes could not be separted due to the thickness of the Si film. In this section, samples with very thin films are considered, so that the theory of Section 6.3.2 can be applied, and the substrate lifetime determined. Four wafers were examined, two annealed at Ibis and two at Harris. The two Harris samples also had very thin epilayers (0.4 and 0.6 μm). The results are listed in Table 6.2. No real trends are evident, but the lifetimes are similar in value to those in Table 6.1. It is surprising that the substrate lifetimes are so short. Although the substrate lifetime is not as directly important to device performance as is the film lifetime, measurement of the substrate lifetime does provide a very handy way of monitoring contamination.

6.4.3 Lifetime measurements of ultra thin films.

An HeCd UV laser operating at 325 nm was obtained to attempt to measure the effective recombination lifetime in the thin SOI films. The absorption coefficient is 1.5×10^6 cm^{-1} at this wavelength, so that the pump beam is essentially absorbed within the top 15 nm. Since the thinnest film under measurement is 0.2 μm, carrier generation in the substrate is negligable for all of the SOI samples. Using the ex-

perimental set up of Fig. 6.2, DBOM measurements were performed on the various SIMOX samples. However, no signal was detected. To minimize the possible effects of surface recombination on the effective lifetime, a thin passivation oxide was grown on several samples, but still, no DBOM signal was detected. As discussed in the theory section, the lack of a DBOM signal is most likely due the reduced number of carriers in the ultrathin film, as well as high level recombination near the surface, due to the very high injection levels. Other approaches are being investigated to overcome these problems. First of all, a longer wavelength pump beam is being investigated to minimize the high level injection recombination effects. Secondly, the feasibility of intersecting the pump and probe beams in a perpindicular manner is being studied.

6.5 Summary

A technique was presented for the contactless measurement of the recombination lifetime in silicon wafers, with special application to SOI wafers. The technique consists of monitoring the absorption of IR light passing through the wafer by excess free carriers. The excess free carriers are generated by a second short wavelength light source. Theory for applying the method to thin and thick film SOI wafers was derived. Attempts to obtain a DBOM signal from ultra thin SOI films were unsuccessful. However, the DBOM approach was applied to the measurements of the substrate lifetime, so that the technique can be used at least as a contamination monitor.

Table 6.1. Lifetime measurements using the DBOM technique. The SIMOX samples were annealed at 1285°C for 6 hours.

Sample	Oxygen Dose	Lifetime
	10^{18} cm^{-2}	μs
MI10	3 x 0.5	0.29
S4419	1.5	0.12
S5109	1.8	0.76
Bulk Si	–	1.13

Table 6.2. Substrate lifetime measurements by applying the DBOM technique to SIMOX wafers with ultra thin Si films. The oxygen dose was 1.8×10^{18} cm^{-2} for all of the samples; however, IB754 is a multiple implant wafer with doses of 0.5, 0.5, and 0.8. The IB wafers were annealed at Ibis while the SOI wafers were annealed at Harris.

Sample	Anneal Temp. and Time	Lifetime
	°C, Hr.	μs
IB754	1310, 5	0.29
IB775	1310, 5	0.17
SOI5-22	1285, 6	0.20
SOI5-40	1285, 6	0.27

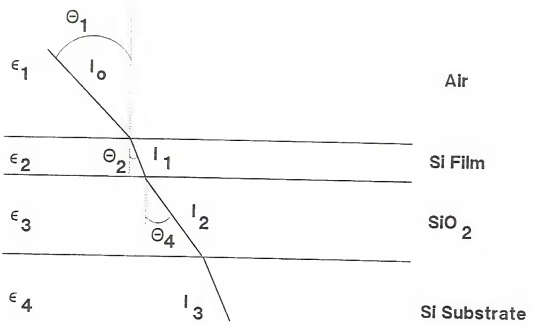


Figure 6.1. Sketch of SOI structure used in calculating I_3/I_o.

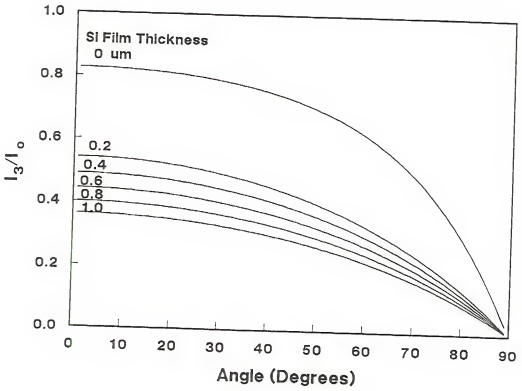


Figure 6.2. Ratio of I_3/I_o for various incident angles and Si film thicknesses.

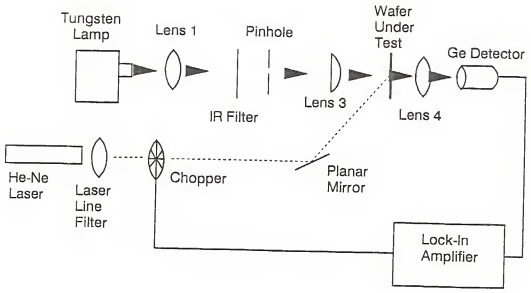


Figure 6.3. Experimental set up for the dual beam optical modulation experiment.

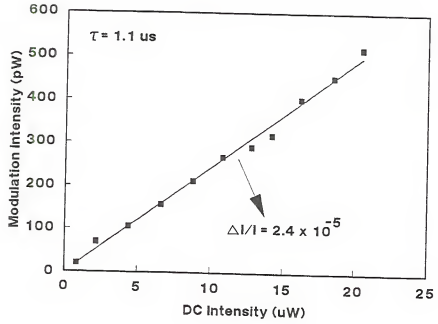


Figure 6.4. Magnitude of the modulation signal as a function of the DC value of the probe beam, showing the expected linear relation.

CHAPTER 7
CONCLUSIONS

The topic of study of this dissertation was the electrically active defects of buried oxide layers formed by oxygen implantation. In order to investigate this buried insulator layer, a high frequency C-V technique was developed to analyze the silicon/insulator/silicon structure. The technique consists of fitting theoretical C-V curves to measured high-frequency C-V curves. From the best fit, the interface state, fixed oxide charge, and doping concentration are determined for each buried oxide interface.

Using this C-V analysis technique, the effects of varying the oxygen implant dose and the post-implant anneal temperature and time were studied. Within the variable range studied, it was found that increasing the anneal temperature strongly reduced the density of all of the defects. The best oxygen implant dose was found to be 1.8×10^{18} cm^{-2}. Increasing the anneal time was found to increase the density of fixed oxide charge, but improve the minority carrier generation lifetime in the Si film. The post-irradiation charge trapping was found to be minimized by increasing the anneal temperature or the anneal time. Changing the implant dose had little effect on the charge trapping. Also, very few interface traps were generated, except for biases for which the electric field was driving the holes to the interface. For the low oxygen dose samples, an increase in the film donor density with X-ray dose was seen. This donor enhancement effect was attributed to the presence of oxide precipitates in the Si film.

A study of the effects of high electric field stress was also conducted. Only samples annealed at 1285°C were considered. It was found that SIMOX oxides had

relatively low threshold fields for Fowler-Nordheim Tunneling. The threshold fields were the same for injection from the substrate. For injection from the film, low-oxygen dose, single-implant samples were found to have enhanced injection, while standard dose samples were found to have reduced injection. The multiple implant samples had very symmetrical injection characteristics. The multiple implant and standard dose samples had net positive oxide charge, while the low-dose single implant sample had a net negative oxide charge. Finally, for all of the samples, the substrate/oxide interface had greater degradation than the film/oxide interface.

Finally, a prototype instrument was developed for the nondestructive evaluation of SIMOX material. The technique consists of generating excess carriers with a pump beam. The transmission of a second beam (with energy that is less than the bandgap) through the wafer is monitored. The free carriers generated by the pump beam will absorb some of the second beam. The degree of attenuation is proportional to the excess carrier lifetime.

REFERENCES

[1] P.K. Vasudev, IEEE Circ. Dev. Mag. 3, 17 (1987).

[2] T.I. Kamins, K.F. Lee, and J.F. Gibbons, IEEE Electron Device Lett. EDL-1, 5 (1980).

[3] S. Kawamura, N. Sasaki, M. Nakano, and M. Takagi, J. Appl. Phys. 55, 1607 (1984).

[4] J.A. Knapp, J. Appl. Phys. 58, 2584 (1985).

[5] M. Haond, D.-P. Vu, A.M. Auguirre, and S. Perret, IEEE Circ. Dev. Mag. 3, 27 (1987).

[6] B.-Y Tsaur, IEEE Circ. Dev. Mag. 3, 12 (1987).

[7] P.P. Pronko, A.W. McCormick, and W. P. Maszara, the 1990 SOS/SOI Technology Conference, Key West, FL.

[8] K. Izumi, M. Doken, and H. Ariyoshi, Electron. Lett. 14, 593 (1978).

[9] P.L.F. Hemment, Mayell-Ondrusz, K.G. Stevens, J.A. Kilner, and J. Butcher, Vacuum 34, 203 (1984).

[10] B.-Y Mao, P.-H. Chang, C.-E. Chen, and H. W. Lam, J. Appl. Phys. 62, 2308 (1987).

[11] D. Hill, P. Fraundorf, and G. Fraundorf, J. Appl. Phys. 63, 4933 (1988).

[12] P.L.F. Hemment, E. Maydell-Ondrusz, K.G. Stephens, J. Butcher, D. Ioannoa, and J. Alderman, Nucl. Inst. Meth. Phys. Res. 209/210, 157 (1983).

[13] C.G. Tuppen, M.R. Taylor, P.L.F. Hemment, and R.P. Arrowsmith, Appl. Phys. Lett. 45, 57 (1984).

[14] O.W. Holland, T.P. Sjoreen, D. Fathy, and J. Narayan, Appl. Phys. Lett. 45, 108 (1984).

[15] T.W. Houston, H. Lu, P. Mei, T.G.W. Blake, L.R. Hite, R. Sundaresan, M. Matloubian, W.E. Bailey, J. Liu, A. Peterson, and G. Pollack, the 1989 SOS/SOI Technology Conference, Stateline, NV 1989.

[16] W.F. Kraus and J.C. Lee, the 1989 SOS/SOI Technology Conference, Stateline, NV 1989.

[17] G.T. Goeloe, G.A. Hanidu, and K.H. Lee, presented at the 1990 Nuclear and Space Radiation Effects Conference, Reno, NV.

[18] G.K. Celler, A. Kamagar, H.-I. Cong, R.L. Field, S.J. Hillenius, W.S. Lindenberger, and L.E. Trimble, the 1989 SOS/SOI Technology Conference, Stateline, NV 1989.

[19] B.-Y Mao, P.-H Chang, H.W. Lam, B.W. Shen, and J.A. Keenan, Appl. Phys. Lett. 48, 108 (1986).

[20] L. Jastrzebski and A.C. Ipri, IEEE Electron Device Lett. EDL-9, 151 (1988).

[21] A. Mogro-Campero, R.P. Love, N. Lewis, E.L. Hall, and M.D. McConnel, J. Appl. Phys. 60, 2103 (1986).

[22] M. Yoshimi, H. Hazama, M. Takahashi, S. Kambayashi, T. Wada, K. Kato, and H. Tango, IEEE Trans. Electron Devices 36, 493 (1989).

[23] J. C. Sturm, K. Tokunaga, and J.P. Colinge, IEEE Electron Device Lett. EDL-9, 460 (1988).

[24] J.P. Colinge, IEEE Electron Device Lett. EDL-7, 244 (1986).

[25] M. Yoshimi, M. Takahashi, T. Wada, K. Dato, S. Kambayashi, M. Kemmochi, and K. Natori, IEEE Trans. on Electron Devices 37, 2015 (1990).

[26] A.H. Van Ommen, B.H. Koek, and M.P.A Viegers, Appl. Phys. Lett. 49, 628 (1986).

[27] C.K. Celler, P.L.F. Hemment, K.W. West, and J.M. Gibson, Appl. Phys. Lett. 48, 532 (1986).

[28] B.-Y Mao, M. Matloubian, C.-E. Chen, R. Sundaresan, and C. Slawinski, IEEE Elect. Dev. Lett. EDL-8, 306 (1987).

[29] B.-Y Mao, R. Sundaresan, C.-E. Chen, M. Matloubian, and G. Pollack, IEEE Trans. on Electron Devices 35, 629 (1988).

[30] P.K. McLarty, D.E. Ioannou, and J.P. Colinge, IEEE Electron Device Lett. EDL-9, 545 (1988).

[31] L. Jastrzebski and R. Soydan, the 1988 SOS/SOI Technology Workshop, St. Simons Island, GA.

[32] J. Vanhellemont H.E. Maes, and A. DeVeirman, J. Appl. Phys. 65, 4454 (1989).

[33] S.I. Raider and R. Flitsch, in The Physics of SiO2 and its Interfaces, edited by S.T. Pantelides (Pergamon, New York, 1978), p. 384.

[34] P.J. Grunthaner, M.H. Hecht, F.J. Grunthaner, and N.M. Johnson, J. Appl. Phys. 61, 629 (1986).

[35] E.H. Snow, A.S. Grove B.E. Deal, and C.T. Sah, J. Appl. Phys. 36, 1664 (1965).

[36] P.M. Lenahan and P.V. Dressendorfer, J. Appl. Phys. 55, 3495 (1984).

[37] M. Knoll, D. Braung, and W.R. Fahrner, IEEE Trans. Nucl. Sci. NS-29, 1471 (1982).

[38] E.H. Nicollian and J.R. Brews, MOS Physics and Technology, (Wiley, New York, 1981).

[39] P.M. Lenahan and P.V. Dresendorfer, Appl. Phys. Lett., 41, 542 (1982).

[40] N.M. Johnson, D.K. Biegelson, M.D. Moyer, and S.T. Chang, Appl. Phys. Lett., 43, 563 (1983).

[41] S.M. Sze, Semiconductor devices, (Wiley, New York, 1981, 2 ed.).

[42] J. Shewchun, R.A. Clarke, and V.A.K. Temple, IEEE Trans. Electron Devices ED-19, 1044 (1972).

[43] K. Nagai, T. Sekigawa, and Y. Hayashi, Solid-State Electron. 28, 789 (1985).

[44] M. Zerbst, A. Angew. Phys. 22, 30 (1966).

[45] W. Kaiser, H.L. Frisch, and H. Reiss, Phys. Rev., 112, 1546 (1958).

[46] V. Cazcarra and P. Zunino, J. Appl. Phys., 51, 4206 (1980).

[47] S. Cristoloveanu, S. Garnder, C. Jasuuaud, J. Margail, A.J. Aurberton-Herve, and M. Bruel, J. Appl. Phys. **62** (1987).

[48] P.O. Hahn and M. Henzler, J. Vac. Sci. Technol. A2, 574 (1984).

[49] B.-Y. Mao, P.-H. Chang, H.W. Lam, and J.A. Keenan, Appl. Phys. Lett. 48, 794 (1986).

[50] T.I. Kamins and S.Y. Chiang, J. Appl. Phys. 58, 2559 (1985).

[51] M. Delfino, M. Jaczynski, A.E. Morgan, C. Vorst, M.E. Lunnon, and P. Maillot, J. Electrochem. Soc. 134, 2027 (1987).

[52] F.T. Brady, S.S. Li, and W.A. Krull, J. Electronic Mat. 18 385 (1989).

[53] B.-Y Tsaur, J.C.C. Fan, G.W. Turner, and D.J. Silversmith, Electron Device Letters EDL-3, 195 (1982).

[54] G.E. Davis, L.R. Hite, T.G.W. Blake, C.-E. Chen, H.W. Lam, and R. DeMoyer, IEEE Trans. on Nuclear Science NS-32, 4432 (1985).

[55] B. Tsaur, V.J. Sferrino, H.K. Choi, C.K. Chen, R.W. Mountain, J.T. Shott, W.M. Shedd, D.C. LaPierre, and R. Blanchard, IEEE Trans. on Nuclear Science NS-33, 1372 (1986).

[56] W.A. Krull, J.F. Buller, G.V. Rouse, and R.D. Cherne, IEEE Circuits and Devices Magazine 3, 20 (July 1987).

[57] B.Y. Mao, C.-E. Chen, G. Pollach, H.L. Hughes, and G.E. Davis, IEEE Trans. on Nuclear Science NS-34, 1692 (1987).

[58] J.F. Buller, W.A. Krull, and R.D. Cherne, the 1988 HEART Conference, Patrick's Air Force Base, FL.

[59] D.G. Platteter and T.F. Cheek, IEEE Trans. on Nuclear Science NS-35, 1350 (1988).

[60] L.J. Palkuti, P. Ling, P. Leonov, H. Kawayoshi, R. Ormond, and J. Yuan, IEEE Trans. on Nuclear Science NS-35, 1653 (1988).

[61] M. Matloubian, E.J. Zorinsky, and D.B. Spratt, IEEE Trans. Nuclear Science NS-35, 1650 (1988).

[62] T.D. Stanley, IEEE Trans. on Nuclear Science," NS-35, 1346 (1988).

[63] G.A. Ausman and F.B. McLean, Apl. Phys. Lett. 26, 173 (1975).

[64] R.C. Hughes, Phys. Rev. Lett. 30, 1333 (1973).

[65] H.E. Boesch, F.B. McClean, J.M. McGarrity, and G.A. Ausman, IEEE Trans. Nuclear Science NS-22, 2163 (1975).

[66] M.R. Shaneyfelt, J.R. Schwank, D.M. Fleetwood, P.S. Winokur, K.L Hughes, and F.W. Sexton, IEEE Trans. Nuclear Science NS-37, 1632 (1990).

[67] N.S. Saks and D.B. Brown, IEEE Trans. Nuclear Science NS-37, 1624 (1990).

[68] Z. Shanfield and M.M. Moriwaki, IEEE Trans. on Nuclear Science NS-34, 1159 (1987).

[69] P.J. McWhorter, P.S. Winokur, and R.A. Pastorek, IEEE Trans. Nuclear Science NS-35, 1154 (1988).

[70] P.S. Winokur, in Ionizing Radiation Effects in MOS Devices and Circuits, ed. by T.P. Ma and P.V. Dressendorfer (Wiley, New York, 1989), p. 333.

[71] F.T. Brady, S.S. Li, D.E. Burk, and W.A. Krull, Appl. Phys. Lett. 52, 886 (1988).

[72] H.E. Boesch, T.L. Taylor, L.R. Hite, and W.E. Bailey, IEEE Trans. Nuclear Science NS-37, 1982 (1990).

[73] C.A. Pennise and H.E. Boesch, IEEE Trans. Nuclear Science NS-37, 1990 (1990).

[74] P.V. Dressendorfer, in Ionizing Radiation Effects in MOS Devices and Circuits, edited by T.P. Ma and P.V. Dressendorfer (Wiley, New York, 1989), pp. 354-359.

[75] F.T. Brady, W.A. Krull, and S.S. Li, IEEE Trans. Nuclear Science Vol. NS-36, No. 6, pp. 2187-2191 (1989).

[76] F.T. Brady, S.S. Li, and W.A. Krull, Solid State Electronics **33**, 1643 (1990).

[77] M. Guerra, in the Proceedings of the Fourth International Symposium on Silicon-on-Insulator Technology and Devices, ed. By D.N. Schmidt, in Montreal, Quebec, Canada, May 1990, pp. 21-48.

[78] Z.A. Weinberg, Solid State Electron. 20, 11 (1977).

[79] S.J. Oh and Y.T. Yeow, Solid State Electron. 32, 507 (1989).

[80] D.J. DiMaria, Appl. Phys. Lett. 51, 655 (1987).

[81] C. C.-H Hsu, T. Nishida, and C.-T. Sah, J. Appl. Phys. 63, 5882 (1988).

[82] J.F. Buller, W.A. Krull, and G.W. Lake, the 1986 SOS/SOI Technology Workshop, Captiva Island, FL.

[83] P. Roitman, M. Edelstein, S. Krause, and S. Visitserngtrukul, the 1990 SOS/SOI Technology Conference, Key West, FL.

[84] P.J. McMarr, B.J. Mrstik, M.S. Barger, G. Bowden, and J.R. Blanco, J. Appl. Phys. 67, 7211 (1990).

[85] ANSI/ASTM F 391-78, 1979 Annual Book of ASTM Standards, Part B, American Society for Testing and Materials, Philadelphia, 1979, p. 770.

[86] D.L. Polla, IEEE Electron Device Lett. EDL-4, 185 (1983).

[87] Z.G. Ling, P.K. Ajmera, M. Anselment, and L.F. DiMauro, Appl. Phys. Lett. 51, 1445 (1987).

[88] J. Waldmeyer, J. Appl. Phys. 63, 1977 (1988).

[89] T.S. Moss, "Optical Properties of Semiconductors," Academic Press, New York, 1959).

BIOGRAPHICAL SKETCH

Frederick Brady was born in Trenton, New Jersey on October 1, 1963. After graduating from Bethlehem Catholic High School, he entered the New Mexico Institute of Mining and Technology (located in Socorro) in 1981. In June 1985, he received the Bachelor of Science degree from the Department of Physics at New Mexico Tech. He then enrolled in the graduate electrical engineering program at the University of Florida, receiving the M.S. and Ph.D degrees in December 1987 and May 1991, respectively. During his Ph.D research he spent two summers as an associate engineer at Harris Semiconductor, conducting research on the radiation hardness of SIMOX buried oxides. In March 1991, he began work at IBM Federal Systems Division in Manassas, Virginia as a Development Staff Engineer, involved in the characterization of SOI materials and devices.

I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

Sheng S. Li, Chairman
Professor of Electrical Engineering

I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

Dorothea E. Burk
Professor of Electrical Engineering

I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

Robert M. Fox
Assistant Professor of Electrical Engineering

I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

Arnost Neugroshel
Professor of Electrical Engineering

I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

Kevin Jones
Assistant Professor of Materials
Science and Engineering

This dissertation was submitted to the Graduate Faculty of the College of Engineering and to the Graduate School and was accepted as partial fulfillment of the requirements for the degree of Doctor of Philosophy.

May 1991

Winfred M. Phillips
Dean, College of Engineering

Madelyn M. Lockhart
Dean, Graduate School